Dr. Bernd Dielacher

Director of Business Development at EV Group (EVG)

Stacking the Future: The Critical Role of Wafer Bonding in Next-Generation Interconnect Scaling

Biography

Dr. Bernd Dielacher leads global business development initiatives at EVG. With a strong background in technology and market analysis, business intelligence, and product marketing, he actively contributes to the company's technology roadmaps and supports the development of next-generation products across EVG's core platforms — including wafer bonding, lithography, and nanoimprint.

Prior to this role, he served as Business Development Manager, with a focus on heterogeneous 3D integration, MEMS, biomedical applications, and power device markets.

Dr. Dielacher holds a Master's degree in Microelectronics from the Vienna University of Technology and a PhD in Biomedical Engineering from ETH Zurich.

Dr Taku Hanna

Senior Manager at the Institute of Advanced Technology, ULVAC

Technology scaling evolution of interposer interconnects forglass core and high-density polymer RDL based on plasma dry processes

As Moore's Law approaches its limits, heterogeneous integration technology is gaining significant attention. In particular, "3D chiplet integration," which combines front-end and back-end processes, is seen as a promising new architecture. Advancing this technology requiresglass core substrates with through-glass vias (TGV) and high-density redistribution layer (RDL) interposers. However, glass substrates withTGV face challenges“SEWARE” from multi-stacked build-up (BU) films.Meanwhile, stacked photo-imageable dielectric (PID) layers as RDLs on a glass substrate gives warpage and cracking due to CTE mismatch and also waviness of the RDLs from spin-on materials. This work reports initial experiments addressing these issues: developing Cu-TGV wiring usingsputtering technology for glass substrates, and plasma etching technology for PIDs with good aspect ratio and fine patterns to improveRDL performance. The thickness of the glass core is 430 μm (size : 50 mm by 40 mm), and the TGV has a cross-shaped structure. The top diameterand constriction diameter are 80 μmφ and 55 μmφ, respectively. Therefore, the aspect ratio is approximately 5 to 7. Double-sided deposition on this glass core was performed by PVD sputtering. After PVD deposition of Ti 200 nm and Cu 2000 nm, Cu electroplating was carried out, resulting in completely filled Cu TGVs. This suggests that introducing the sputtering process can reduce thermal budget risks while ensuring good adhesion. Next, using plasma dry etching, vertical etching of PID with a line and space of 2.5 μm, an etching depth of 4.3 μm, and an aspect ratio of 1.72 was achieved. This presents a new fine processing technology for multilayer RDL interposer processes.

Biography

Taku Hanna joined ULVAC in 2017. He earned a Ph.D. in Engineering with a focus on inorganic material development from the Tokyo Institute of Technology. He has been involved in the development of highly-sensitive hydrogen detectors, alloys, and oxide semiconductor materials, as well as oxide semiconductor TFT devices. Currently, he is working as a Senior Manager in the fields of advanced packaging technology and power semiconductors at the Institute of Advanced Technology at ULVAC. In this role, he is engaged in the research and development of semiconductor manufacturing equipment, including sputtering and etching equipment.

Dr. Yi Zhao

Founder and Chief Scientist, Zhuhai Silicon Chip Technology Ltd.

New Paradigm in Advanced Packaging: EDA as a Strategic Bridge for Co-Design and Manufacturing, Bridging the Full 2.5D/3D-IC “Design-Simulation-Verification” Flow

n the post-Moore era, as single-chip performance improvements encounter bottlenecks, Chiplet and 2.5D/3D-IC advanced packaging technologies have become the core engines driving continuous innovation in the semiconductor industry. This technological revolution not only reshapes the architectural design philosophy of chips but also imposes disruptive requirements across the entire industry chain, particularly for upstream EDA tools.

Today, the industry no longer faces challenges from isolated technical points but confronts systemic ecosystem dilemmas: How can full-flow co-optimization from chiplet-interconnect design to system-in-package be achieved? How can we balance power, cost, and reliability while ensuring peak performance? How can we break down data barriers between design, manufacturing, and testing?

As a pioneer in advanced packaging EDA, SiChip Technology will introduce the 3Sheng Integration stacked-IC EDA platform, which is driven by a dual-loop co-optimization framework: “chiplet–interposer–Co-packaged Design” and “Performance-Cost-Testability Co-Optimization.”It has established a full-flow toolchain comprising five core centers: 3Sheng Zenith (Architecture Design) – 3Sheng Ranger (Physical Implementation) – 3Sheng Ocean (Multi-die DFT) – 3Sheng Volcano (Co-Simulation) – 3Sheng Stratify (Multi-die Physical Verification)(LVS and DRC), building a new advanced packaging ecosystem through technological innovation and Co-optimization.

Biography

Holding a Ph.D. from the University of Southampton, UK, under the supervision of Royal Society Fellow Professor Bashir Hashimi, he embarked on 2.5D/3D stacked IC design research in 2008 as part of one of the world’s earliest pioneering research teams exploring advanced chip architecture methodologies, having collaborated with IMEC for 3D-IC technology validation. With 15 years of dedicated R&D in 3D integrated circuit design, he has published several excellent papers and was awarded the VLSI-SOC Best Paper. Currently serving as Founder and Chief Scientist at Zhuhai Silicon Chip Technology Ltd., he has been a major leader of national research initiatives. He directs the team in developing self-proprietary 2.5D/3D Stacked IC EDA tools, enabling critical advancements in the semiconductor industry through backend full-flow EDA tools and solutions.

Inohara Masahiro

Memory packaging Development Department, Memory Division, KIOXIA Corporation

Accelerating the Evolution of NAND Flash Memory with Bonding Technologies

NAND flash memory was invented in 1987 by KIOXIA (formerly known as TOSHIBA Memory) and has been evolving for about four decades. Continuous improvement in bit density has been achieved through 2D and subsequent 3D scaling, overcoming trade-offs in performance. While 3D scaling will continue to drive higher bit density, the transition from a monolithic die to a multi-die approach contributes to improved performance with fewer constraints. CBA (CMOS directly Bonded to Array) technology, introduced in the 8th generation of BiCS FLASH, enhances the flexibility of process optimization and improves the lead time for new products by separating a monolithic die into the CMOS die and the array die, and bonding them through wafer-to-wafer hybrid bonding. Expanding the range of bonding technologies being introduced will help us meet increasing requirements such as higher bandwidth, more functions in memory, and lower power consumption as well as higher bit capacity. Multi die stacking of CMOS dies provides greater flexibility for computing functions in memory. Multi die stacking of array dies accelerates the increase in bit density per unit area. Die-to-wafer(die-to-die) bonding eliminates restrictions on chip sizes that can be bonded, and it allows for the bonding KGD (Known Good Die) after testing. In this talk, we will review process options for bonding technology and discuss potential advantages of multi die bonding in various applications.

Biography

Masahiro Inohara is the Chief Specialist at KIOXIA Corporation, currently involved in advanced packaging development and planning. He has over 30 years of experience in the semiconductor industry and began his career as a process and device development engineer for logic, SRAM, and analog ICs at TOSHIBA Corporation (the original company from which KIOXIA spun out). After serving for 2 years in the corporate strategy department, he moved to NAND flash memory division, where he developed 3D NAND flash memory across several generations, including hybrid bonding technology. He holds over 54 patents and has authored more than 14 publications. He received his B.S. and M.S. degrees in engineering science from Tsukuba University, Ibaraki, Japan, in 1991 and 1993, respectively.

Dr. Mushuan Chan

CRD Director

High Layer RDL Process Technology for Heterogeneous Integration Package.

The relentless demand for increased functionality, higher performance, and smaller form factors in semiconductor devices has propelled heterogeneous integration chip to the forefront of advanced packaging solutions. The interconnect density and complexity have become a primary bottleneck. We present the development of high-layer Redistribution Layer (RDL) process technology specifically designed to enable next-generation advance packages. When more redistribution layers are implement to the fine line/space, it may cause the worse topography and effect the following process. How to perform polymer dielectric material planarization will be the challenge. The process utilizes an advanced lithography and copper electroplating scheme to consistently achieve fine line/space (L/S) features down to 2/2 μm with multi layers.

Biography

Mu-Hsuan Chan received Ph.D in Materials Science & Engineering from National Chung Hsing University. She joins SPIL in 2011 over 10 years of job experience in advance packaging technologies , especially focusing on wafer level assembly technologies.

Dr Sajay BG

Scientist at the Institute of Microelectronics (IME), A*STAR, Singapore

Heterogeneously Integrated Wafer-Level processed Co-Packaged Optical Engines for Next-Gen AI/ML Data Centers

The rapid growth of data center traffic and AI/ML workloads is driving the demand for high-bandwidth, low-latency optical connectivity. To address this, we have developed a 300 mm fan-out wafer-level packaging (FOWLP) platform that heterogeneously integrates silicon photonics ICs (PIC), electronic ICs (EIC), and lasers into compact co-packaged optical engines with bandwidth of 800G/1.6T/3.2T/6.4T and beyond. This platform delivers a cost-effective and scalable solution for high-volume manufacturing, offering clear advantages over 2.5D interposer and 3D-TSV technologies. We have qualified multiple through-package interconnect approaches to connect the frontside and backside RDL of the package, including laser-drilled through-mold vias, discrete prefabricated substrate-based vias, and fine-pitch through-glass vias, providing ultra-low-loss signal transmission. The process integration flow is carefully designed to preserve key PIC features such as edge and vertical optical I/Os. Several architectures were demonstrated and benchmarked against performance and integration metrics. In addition, a hybrid-bonded optical engine platform is under development to further enhance bandwidth density and energy efficiency. Our packaging solutions enable high-bandwidth PIC–EIC interconnects in a compact, cost-effective, and scalable form factor. Modeling and experimental results shows the packaging interconnects supports PAM4 transmission up to 448 Gbps per lane, with robust mechanical and thermal performance, supporting the next generation of AI/ML Data Centers and High-Performance Computing deployments.

Biography

Dr. Sajay BG is a Scientist at the Institute of Microelectronics (IME), A*STAR, Singapore, with over 19 years of experience in the semiconductor industry and research. He earned his Ph.D. in Electrical and Electronic Engineering (Microelectronics) from Nanyang Technological University, Singapore, and a Master's degree in Mechatronics from the National University of Singapore. Prior to joining IME, he gained industry experience at STATS ChipPAC Ltd, Hewlett-Packard Ltd, and Siltronic Singapore Pte Ltd, specializing in wafer-level packaging and MEMS technologies. At IME, Dr. Sajay focuses on electronic-photonic heterogeneous integration and semiconductor system-in-package (SiP) technologies, successfully demonstrating advanced optical engine package platforms for AI/HPC applications.

Dr. Kathy Yan

Director of New Technology & System Integration, Advanced Packaging and Test at TSMC HQ

From Cloud AI to Edge AI: Driving Innovation with Advanced Packaging

Biography

Kathy Yan is the Director of New Technology & System Integration, Advanced Packaging and Test at TSMC HQ, with 20+ years of experience in advanced packaging R&D at Intel (US), Medtronic, and TSMC.

CoWoS-R organic interposer technology owner at TSMC, responsible for technology architecture definition, technology scaling and expansion, process and material development. Her research focuses on electrical simulation for product SI/PI optimization, design rules advancement, and thermal mechanical stress validation. She also specialized in innovated package-level and system-level thermal solution. Previously, she leads new product co-development across various packaging technologies, includes InFO-POP, InFO-oS, InFO-SOW, and CoWoS-S. She is also tsmc HBM technology program manager for 3D Fabric Alliance.

Kathy Yan hold a Ph.D. in Electrical Engineering and a Master's in Material Science from Auburn University, and a B.S. in Electrical Engineering from Shanghai Jiaotong University. Filed over 50 patents across the US, Germany, Taiwan, and China..

Dr. Takenori Fujiwara

Chief Research Associate in Electric & Imaging Materials Research Labs at Toray

Polymer bonding technology for semiconductor advanced PKG

Introduction of the latest development overview of polymer bonding technologies such as polymer hybrid bonding, carrier bonding with mass transfer technology application for µLED and photonics, etc., direct bonding of TIM for power electronics and polymer sealing bonding materials (MEMS).

Biography

Dr. Takenori <Ken> Fujiwara, a PhD holder of Material Engineering from Nagoya University, has more than 25 years of experience in IT related materials such as microelectronics, photonics, display technologies, high-heat-resistant polymers, Spin on glass and legacy materials used in packaging businesses. Along with his technical experience, he has published numerous technical papers and patents as an engineer of academia.

His involvements in various consortiums and symposiums such as Tsukuba Power Electronics Constellations, IME consortium in Singapore and SMTA WLPS' Technical committee chair has gained enormous amount of trust and partnership with many packaging engineers around the globe. The other technical committee: IMAPS(US), EPTC(SG) and NEDIA(JP).

As the Chief Research Associate in Electric & Imaging Materials Research Labs at Toray, he became the inaugural Chief who started-up "Toray Singapore Research Center" in 2022, where he expanded his knowledge of the next generation of packages by working closely with distinguished engineers worldwide.

Dr. Tan Yik Yee

Senior Market and Technology Analyst Yole Intelligence

AI is accelerating the shift to advanced packaging with FOPLP and glass cores.

The semiconductor industry continues to demonstrate strong growth, fuelled by rising demand in AI, automotive, and consumer markets. As conventional scaling approaches encounter physical and economic limits, advanced packaging has become a key enabler for enhancing performance, integration, and miniaturization. Industry focus is now shifting toward next-generation advanced packaging technologies. Solutions such as fan-out panel-level packaging (FOPLP) and glass core substrates are gaining momentum and shaping the future landscape.

Panel-Level Packaging (PLP) is attracting attention for its potential in cost efficiency and high-volume production. Yet, its adoption brings material challenges, particularly in warpage control, thermal stability, and process compatibility. At the same time, glass substrates are being investigated for their excellent dimensional stability and electrical insulation. While promising, glass introduces hurdles in handling, via formation, and integration within existing packaging ecosystems. This presentation will be exploring both emerging technology trends, market drivers, and supply chain dynamics—providing insights into both the opportunities and challenges that will define the path forward for advanced packaging solutions.

Biography

Yik Yee Tan Ph.D. is a Principal Technology & Market Analyst, Semiconductor Packaging & Assembly at Yole Group. Dr. Tan holds a Ph.D. in Engineering from Multimedia University (MMU, Malaysia). She has more than 25 years of experience in semiconductor packaging. Based on her technical expertise and market knowledge, she develops technology & market reports and is engaged in dedicated custom projects.

Prior to Yole, Dr. Tan worked as a failure analyst and interconnect champion at Infineon Technologies (Malaysia) and later as an open innovation senior manager at Onsemi (Malaysia). She published more than 30 papers and hold 4 patents and award winner for IEEE EPS - Regional 10 Contribution Award 2024 and IEEE Malaysia Section – Outstanding Industry Volunteer Award 2024.

Jonathan Abdilla

Director CTO Office at Besi

Hybrid Bonding and Fluxless TCB: Defining the Sub 10µm Interconnect Roadmap for 3D Heterogeneous Integration

The relentless demand for increased computational density and reduced power-per-bit in Artificial Intelligence (AI) and High-Performance Computing (HPC) is pushing scaling to its limits. Achieving ultra-high bandwidth and low power consumption requires moving from micro-bumps to sub 10 µm pitch interconnects. two interconnect technologies stand at the forefront: Die to wafer hybrid bonding and fluxless thermocompression bonding.Fluxless Thermo-Compression Bonding (TCB), an extension of back-end packaging, is a promising solution for the fine-pitch sub 20µm solder-based or Cu-Cu pillar interconnect regime, often targeting the 10 µm to 25 µm pitch window.". The aim is to avoid flux residue which is a critical contaminant limiting pitch scaling in standard TCB.Die to wafer hybrid bonding combining simultaneous Cu-Cu and dielectric-to-dielectric fusion, enables the smallest interconnect pitch (sub 5µm), offers the highest I/O density, and results in a near-zero die-to-die standoff height. This front-end-of-line process provides superior electrical and thermal pathways, but demands the highest level of die bonding equipment in terms of accuracy, cleanliness and throughput.This presentation will highlight and quantify recent advancements in both fields—detailing equipment capability, post-bond analysis, and providing cross-sectional evidence and electrical test data that define the operational boundaries and optimal use cases for each technology. Keywords: Hybrid Bonding (Cu-Cu/Dielectric), Fluxless Thermo-Compression Bonding (TCB), 3D IC, Heterogeneous Integration, Interconnect Scaling, Thermal Management.

Biography

Jonathan has a degree in Mechanical Engineering and an Executive MBA from the University of Malta and a diploma in Computing Information Systems from the University of London. He has 19 years of packaging experience in the semiconductor industry. Before joining BESI, Jonathan worked for STMicroelectronics as process specialist. He then joined BESI taking on roles of Manager for Process Development, Product Manager for Hybrid Bonding and currently Director in the CTO office. He resides on several technical committees for semiconductor packaging conferences.

Dr Fu Chao

Vice General Manager of Wintech-Nano

Lableess Enable High-Quality Development of Singapore Semiconductor

Singapore Semiconductor industry facing challenges in high investments in high-end equipment, limited specialized technical expertise, diversify technological iteration, which often limit the company to achieve optimal R&D performance. Wintech Nano's LABLESS Model exemplifies an innovative paradigm of specialized segmentation in the semiconductor industry, centering on the outsourcing of "essential non-core" R&D testing processes to third-party laboratories. By this means, enterprises are enabled to access impartial, high-efficiency services—including failure analysis, material characterization, and process monitoring—without establishing full-scale in-house labs, with costs reduced by over 60%.
Wintech Nano, which operates "Super Laboratory" in Singapore, Suzhou and other locations. Over 2,000 global clients across the semiconductor value chain—from IC design, Wafer Fab, Packaging and Material sectors. While a transitional "Lab-Lite" model (combining small in-house labs with outsourcing) is currently employed by the industry, testing has been established as an independent sector by LABLESS. Driven by technological innovation, traditional R&D barriers are dismantled by LABLESS model, and a collaborative ecosystem that accelerates innovation and enhances operational efficiency across the Singapore semiconductor industry.

Biography

VP of Wintech Nano-Technology Services Pte. Ltd. Wintech Nano is trusted partner in Singapore Semiconductor industry for more than 21 years, providing analytical services in Material Analysis (MA), Failure Analysis (FA), Reliability Analysis (RA). Fu Chao plays a pivotal role in shaping the company’s strategic direction and operational excellence. He’s responsibilities include overseeing the company’s marketing strategic, and fostering LABLESS collaborations with industry stakeholders. Prior to joining Wintech, he was work in FA department in Agilent/Avago.

David Gani

Director of Packaging R&D at STMicroelectronics

Challenges and Advantages in Panel Level Packaging

Panel level packaging represents a new frontier in semiconductor industry development. It offers significant opportunities to enhance processing efficiency by minimizing unused wafer area and reducing packaging costs—two key drivers behind its evolution. Like any emerging technology, panel level packaging presents both advantages and challenges in its adoption.

This presentation will share STMicroelectronics' experience in implementing panel level packaging, highlighting insights gained from over two years of high-volume production.

Biography

David Gani is Director of Packaging R&D at STMicroelectronics, based in Singapore. With 20 years of experience at ST, he leads a cross-regional team in Singapore and Taiwan, delivering advanced packaging solutions tailored to product functionality and business needs. David spearheads the future packaging strategy and roadmap, with a focus on Chip Scale Packaging technology, ensuring ST remains at the forefront of innovation. He holds over 20 U.S. patents, reflecting his strong contribution to the company's intellectual property portfolio. Prior to joining ST, David worked as a process engineer at PT Unisem Batam. He earned a Mechanical Engineering degree from Gadjah Mada University, Indonesia. Outside of work, he is an avid badminton player and values time with his family.

Dr. Min Woo Rhee

Master, Vice President of Technology, Samsung Electronics

Understanding of Hybrid Bonding Mechanism By Utilizing Molecular Dynamics Simulation Approach

Hybrid bonding has emerged as a promising 3D integration technology for the next generation stacking devices, with the advantages of higher performance and smaller form factor over the conventional micro-bump interconnects. The overall procedures of hybrid bonding that encompass plasma surface treatment, hydration, bonding and annealing are all important steps for successful integration, but detailed mechanisms underlying each process step have not been fully elucidated yet, especially at the atomic level bonding interfaces. Here, we present atomistic-scale modeling procedures of SiO2 and SiCN thin film which are the dielectric materials actively investigated for Cu/dielectrics hybrid bonding applications. The surface models we developed in this work reflect important surface features such as atomic compositions, oxide thickness, surface roughness from various experimental characterization techniques. Reactive molecular dynamics (MD) simulations were then carried out on these models to demonstrate hybrid bonding of dielectric materials and elucidate the surface activation to bonding mechanisms. The plasma-surface interactions of dielectric surfaces presented in our work provide thorough understanding of plasma activated surface topology at the resolution scale that is often hard to reach with the experimental characterization techniques. In addition, the computational workflow represented here may provide a useful guideline for the surface modification process and overcome the time and expense resource constraints by supplementing empirical decisions made from the trial and error based full design of experiment endeavors.

Biography

MINWOO RHEE is Master and Vice President of Technology and leading advanced packaging process and equipment development in Samsung Electronics since 2015. He received the B.Eng., M.S., and Ph.D. degrees in chemical engineering from Sogang University, Seoul, in 1996, 1998, and 2010, respectively and also received Master's degree of management of technology from National University of Singapore (NUS) in 2017. He has been working for more than 23 years in microelectronics packaging research and development for both industry and research institutes and also has extensive experiences in new packaging and material development, numerical modeling, and characterization. From 1999 to 2010, he was with research and development at Amkor Technology, where he was the senior manager and leader of the material characterization, modeling and failure analysis group and resolved lots of chronicle failures and quality issues with worldwide semiconductor companies. Dr. Rhee was a recipient of “the Best Employee of the Year Award in 2009 at Amkor (in R&D section)”. Also he was with the research and development group at Fairchild Semiconductor as a principal engineer, where he developed power device packaging solutions such as automotive three-phase inverter module for high-power electronics, which were successfully applied for mass production for automotive industries. From 2011 to 2015, he was the head of department of IPP (interconnection and packaging program) at Institute of Microelectronics (IME-A*STAR), Singapore and led the advanced packaging group and related industry consortium projects for semiconductor, automotive, oil and gas, deep sea exploration, and aerospace industries. At IME A*STAR he had project-leading experiences of lots of public-funded and industry projects related with material and new packaging development such as MEMS, 3DIC TSV packaging, and power electronics packaging solution for SiC/GaN devices. He is currently Master and vice president of technology and leading advanced packaging equipment research and development in Mechatronics Research, Samsung Electronics since 2015. Dr. Rhee is recipient of the "Future Creator Award" and "DS (Device Solution) Excellence in Technology Award" from Samsung Electronics in 2018. He has authored and co-authored 100+ journal and conference papers and 40+ patents in microelectronics materials and packaging fields.

Hidenori Abe

CTO for semiconductor materials, Resonac Holdings Corporation
Executive director, Electronics Business Headquarters, Resonac Corporation

Advanced Packaging Materials Innovation through Co-creative Evaluation Platform

Advances in equipment and material technology support the cutting-edge semiconductors necessary for the evolution of AI. The emergence of chiplet package structures has led to increased complexity in packaging, making collaboration between materials manufacturers and equipment manufacturers more critical than ever. Resonac, a co-creative chemical company that provides a variety of semiconductor materials such as CMP slurry, etching gas, materials for HBM, epoxy molding compounds, substrate core materials, and more, is advancing materials technology development through open innovation activities. Resonac has started a Packaging Solution Center to propose one-stop solutions for customers and has established the co-creative packaging evaluation platform “JOINT2” with leading companies to accelerate the development of advanced materials, equipment, and substrates for 2.xD and 3D packages. Furthermore, in 2025, the company launched the open innovation initiative "US-JOINT" in Silicon Valley, USA, and launched a new co-creation platform, "JOINT3," in Japan to accelerate technology development through co-creation. This presentation will introduce Resonac's co-creation strategies.

Biography

Hidenori Abe is CTO for semiconductor materials and Executive Director of Electronics Business Headquarters at Resonac. He leads R&D and strategy for electronic materials in semiconductors, substrates, and displays.
Previously, Mr. Abe served as the head of the Electronics R&D Center and Packaging Solution Center, where he contributed to advanced packaging development through open innovation. Notably, in 2021, he directed the launch of JOINT2, a consortium targeting 2.xD and 3D packaging technologies. He also led the launch of "US-JOINT" and "JOINT3" in 2025.
He received a master’s degree in chemical engineering from Tokyo Institute of Technology, Japan, and a master’s degree in the Executive MBA program from the University of Oxford, UK.

Prof. Ali Shakouri

Associate Dean for Research and Innovation, College of Engineering, Purdue University

Thermal Characterization and AI Analytics for 3D Heterogeneous Integrated Circuits

This talk reviews the latest thermal characterization and artificial intelligence-enhanced imaging techniques of devices, integrated circuits, and 3D heterogeneously integrated packages. Complex modules may include multi-layer metallization and copper through-silicon vias. Heat dissipation in such devices requires careful optimization of bonding interfaces and heat sink integration. During operation, minor defects or voids can create hot spots, which, over time, can reduce the chip's performance and reliability. It is advantageous if the integrity of complex ICs could be characterized during manufacturing before complete packaging and powering of the device. Laser heating and transient infrared and thermoreflectance imaging can be used to characterize heat flow in three-dimensional integrated circuits. While inverse problems in heat diffusion are ill-posed, machine learning techniques can be very effective for sub-diffraction far-field imaging and extracting valuable information about buried materials and interfaces.