Dr. Bernd Dielacher

Director of Business Development at EV Group (EVG)

Stacking the Future: The Critical Role of Wafer Bonding in Next-Generation Interconnect Scaling

Biography

Dr. Bernd Dielacher leads global business development initiatives at EVG. With a strong background in technology and market analysis, business intelligence, and product marketing, he actively contributes to the company's technology roadmaps and supports the development of next-generation products across EVG's core platforms — including wafer bonding, lithography, and nanoimprint.

Prior to this role, he served as Business Development Manager, with a focus on heterogeneous 3D integration, MEMS, biomedical applications, and power device markets.

Dr. Dielacher holds a Master's degree in Microelectronics from the Vienna University of Technology and a PhD in Biomedical Engineering from ETH Zurich.

Prof. Dr. Harald Kuhn

Director, Fraunhofer Institute for Electronic Nano Systems ENAS

Scaling AI Infrastructure with Advanced Optical Interconnects

The rapidly evolving landscape of semiconductor technology demands innovative approaches to overcome the challenges of hetero-integration in process technology, test and reliability. This presentation explores key aspects, highlighting three critical areas for a wide range of micro assembly applications:

One of the pivotal elements in the fabrication of heterogeneous integrated systems is wafer bonding technology. This section delves into the complexities and advancements of these wafer to wafer bonding techniques, highlighting their critical function in heterogeneous integration using the example of chemical mechanical planarization (CMP). It encompasses an examination of the latest technologies and their impact in semiconductor devices.

The integration of digital twins and artificial intelligence within CMP as an example is another key area of focus. This entails an exploration of how AI-driven digital twins enhance process control and optimization in semiconductor manufacturing, resulting in more precise control and increased efficiency in CMP processes.

Ensuring the quality and reliability of heterogeneous integrated systems remains paramount concern. This segment addresses the distinct challenges and established procedures for testing and ensuring the long-term reliability of these advanced semiconductor devices. It will discuss the methods for verifying functionality and durability in these complex systems.

By examining these key areas, this presentation provides valuable insights into the intricacies and solutions with hetero-integration, driving innovation, research and future advancements for use with the next generation semiconductor test applications. The increasing complexity requires new solutions for testing, e.g., DfT, KGD up to advanced test systems.

David Gani

Director of Packaging R&D at STMicroelectronics

Challenges and Advantages in Panel Level Packaging

Panel level packaging represents a new frontier in semiconductor industry development. It offers significant opportunities to enhance processing efficiency by minimizing unused wafer area and reducing packaging costs—two key drivers behind its evolution. Like any emerging technology, panel level packaging presents both advantages and challenges in its adoption.
This presentation will share STMicroelectronics' experience in implementing panel level packaging, highlighting insights gained from over two years of high-volume production.

Biography

David Gani is Director of Packaging R&D at STMicroelectronics, based in Singapore. With 20 years of experience at ST, he leads a cross-regional team in Singapore and Taiwan, delivering advanced packaging solutions tailored to product functionality and business needs. David spearheads the future packaging strategy and roadmap, with a focus on Chip Scale Packaging technology, ensuring ST remains at the forefront of innovation. He holds over 20 U.S. patents, reflecting his strong contribution to the company's intellectual property portfolio. Prior to joining ST, David worked as a process engineer at PT Unisem Batam. He earned a Mechanical Engineering degree from Gadjah Mada University, Indonesia. Outside of work, he is an avid badminton player and values time with his family.

Inohara Masahiro

Memory packaging Development Department, Memory Division, KIOXIA Corporation

Accelerating the Evolution of NAND Flash Memory with Bonding Technologies

NAND flash memory was invented in 1987 by KIOXIA (formerly known as TOSHIBA Memory) and has been evolving for about four decades. Continuous improvement in bit density has been achieved through 2D and subsequent 3D scaling, overcoming trade-offs in performance. While 3D scaling will continue to drive higher bit density, the transition from a monolithic die to a multi-die approach contributes to improved performance with fewer constraints. CBA (CMOS directly Bonded to Array) technology, introduced in the 8th generation of BiCS FLASH, enhances the flexibility of process optimization and improves the lead time for new products by separating a monolithic die into the CMOS die and the array die, and bonding them through wafer-to-wafer hybrid bonding. Expanding the range of bonding technologies being introduced will help us meet increasing requirements such as higher bandwidth, more functions in memory, and lower power consumption as well as higher bit capacity. Multi die stacking of CMOS dies provides greater flexibility for computing functions in memory. Multi die stacking of array dies accelerates the increase in bit density per unit area. Die-to-wafer(die-to-die) bonding eliminates restrictions on chip sizes that can be bonded, and it allows for the bonding KGD (Known Good Die) after testing. In this talk, we will review process options for bonding technology and discuss potential advantages of multi die bonding in various applications.

Dr. Tan Yik Yee

Senior Market and Technology Analyst Yole Intelligence

AI is accelerating the shift to advanced packaging with FOPLP and glass cores.

The semiconductor industry continues to demonstrate strong growth, fuelled by rising demand in AI, automotive, and consumer markets. As conventional scaling approaches encounter physical and economic limits, advanced packaging has become a key enabler for enhancing performance, integration, and miniaturization. Industry focus is now shifting toward next-generation advanced packaging technologies. Solutions such as fan-out panel-level packaging (FOPLP) and glass core substrates are gaining momentum and shaping the future landscape.

Panel-Level Packaging (PLP) is attracting attention for its potential in cost efficiency and high-volume production. Yet, its adoption brings material challenges, particularly in warpage control, thermal stability, and process compatibility. At the same time, glass substrates are being investigated for their excellent dimensional stability and electrical insulation. While promising, glass introduces hurdles in handling, via formation, and integration within existing packaging ecosystems. This presentation will be exploring both emerging technology trends, market drivers, and supply chain dynamics—providing insights into both the opportunities and challenges that will define the path forward for advanced packaging solutions.

Biography

Yik Yee Tan Ph.D. is a Principal Technology & Market Analyst, Semiconductor Packaging & Assembly at Yole Group. Dr. Tan holds a Ph.D. in Engineering from Multimedia University (MMU, Malaysia). She has more than 25 years of experience in semiconductor packaging. Based on her technical expertise and market knowledge, she develops technology & market reports and is engaged in dedicated custom projects.

Prior to Yole, Dr. Tan worked as a failure analyst and interconnect champion at Infineon Technologies (Malaysia) and later as an open innovation senior manager at Onsemi (Malaysia). She published more than 30 papers and hold 4 patents and award winner for IEEE EPS - Regional 10 Contribution Award 2024 and IEEE Malaysia Section – Outstanding Industry Volunteer Award 2024.

Dr. Mushuan Chan

CRD Director

High Layer RDL Process Technology for Heterogeneous Integration Package.

The relentless demand for increased functionality, higher performance, and smaller form factors in semiconductor devices has propelled heterogeneous integration chip to the forefront of advanced packaging solutions. The interconnect density and complexity have become a primary bottleneck. We present the development of high-layer Redistribution Layer (RDL) process technology specifically designed to enable next-generation advance packages. When more redistribution layers are implement to the fine line/space, it may cause the worse topography and effect the following process. How to perform polymer dielectric material planarization will be the challenge. The process utilizes an advanced lithography and copper electroplating scheme to consistently achieve fine line/space (L/S) features down to 2/2 μm with multi layers.

Biography

Mu-Hsuan Chan received Ph.D in Materials Science & Engineering from National Chung Hsing University. She joins SPIL in 2011 over 10 years of job experience in advance packaging technologies , especially focusing on wafer level assembly technologies.

Dr. Takenori Fujiwara

Biography

Dr. Takenori <Ken> Fujiwara, a PhD holder of Material Engineering from Nagoya University, has more than 25 years of experience in IT related materials such as microelectronics, photonics, display technologies, high-heat-resistant polymers, Spin on glass and legacy materials used in packaging businesses. Along with his technical experience, he has published numerous technical papers and patents as an engineer of academia.

His involvements in various consortiums and symposiums such as Tsukuba Power Electronics Constellations, IME consortium in Singapore and SMTA WLPS' Technical committee chair has gained enormous amount of trust and partnership with many packaging engineers around the globe. The other technical committee: IMAPS(US), EPTC(SG) and NEDIA(JP).

As the Chief Research Associate in Electric & Imaging Materials Research Labs at Toray, he became the inaugural Chief who started-up "Toray Singapore Research Center" in 2022, where he expanded his knowledge of the next generation of packages by working closely with distinguished engineers worldwide.