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EPTC2024 Professional Development Course #1

Chiplet, Heterogeneous Integration, and Co-Packaged Optics

John H Lau

Unimicron Technology Corporation

Abstract: Chiplet is a chip design method and heterogeneous integration (HI) is a chip packaging method. HI uses packaging technology to integrate dissimilar chips, photonic devices, and/or components (either side-by-side, stacked, or both) with different sizes and functions, and from different fabless design houses, foundries, wafer sizes, and feature sizes into a system or subsystem on a common package substrate. For the next few years, we will see more implementations of a higher level of chiplet designs and HI packaging, whether it is for cost, time-to-market, performance, form factor, or power consumption. In this lecture, the introduction, recent advances, and trends in chiplet design and HI packaging will be presented. Silicon photonics are the semiconductor integration of EIC and PIC on a silicon substrate (wafer) with complementary metal-oxide semiconductor (CMOS) technology. On the other hand, co-packaged optics (CPO) are heterogeneous integration packaging methods to integrate the optical engine (OE) which consists of photonic ICs (PIC) and the electrical engine (EE) which consists of the electronic ICs (EIC) as well as the switch ASIC (application specific IC). The advantages of CPO are: (a) to reduce the length of the electrical interface between the OE/EE (or PIC/EIC) and the ASIC, (b) to reduce the energy required to drive the signal, and (c) to cut the latency which leads to better electrical performance.

Part A: **Chiplet Design and Heterogeneous Integration Packaging**

- System-on-Chip (SoC)
- Why Chiplet Design?
- Chiplet Design and Heterogeneous Integration Packaging
  - Chip partition and Heterogeneous Integration
  - Chip split and Heterogeneous Integration
  - Advantages and Disadvantages
  - Examples
- Lateral Communication between Chiplets (e.g., Bridges)
  - Bridge Embedded in Build-up Package Substrate
  - Bridge Embedded in Fan-Out EMC with RDLs
  - UCIe
  - Hybrid Bonding Bridge
- Chiplet Design and Heterogeneous Integration Packaging - Multiple System and Heterogeneous Integration
  - Multiple System and Heterogeneous Integration with Package Substrate (2D IC Integration)
  - Multiple System and Heterogeneous Integration with Thin Film layer on the Package Substrate (2.1D IC Integration)
  - Multiple System and Heterogeneous Integration with TSV-less (Organic) Interposer (2.3D IC Integration)
  - Multiple System and Heterogeneous Integration with Passive TSV-Interposer (2.5D IC Integration)

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- Multiple System and Heterogeneous Integration with Active TSV-Interposer (3D IC Integration)

- Summary
- Potential R&D Topics in Chiplet Design and Heterogeneous Integration Packaging
- Trends in Chiplet Design and Heterogeneous Integration Packaging

Part B: Co-Packaged Optics (CPO)

- Silicon Phontonic
- Data Centers
- Optical Transceivers
- Optical Engine (OE) and Electrical Engine (EE)
- OBO (on-board optics)
- NPO (near-board optics)
- CPO (co-packaged optics)
- Integration of the PIC and EIC
- 2D Heterogeneous Integration of PIC and EIC
- 2D Heterogeneous Integration of ASIC Switch, PIC and EIC
- 2D Heterogeneous Integration of ASIC Switch, PIC and EIC with Bridges
- 3D Heterogeneous Integration of PIC and EIC
- 3D Heterogeneous Integration of ASIC Switch, PIC and EIC
- 3D Heterogeneous Integration of ASIC Switch, PIC and EIC with Bridges
- Heterogeneous Integration of ASIC Switch, PIC and EIC on Glass Substrate
- Summary
- Trends in Co-Packaged Optics

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Biography:

John H Lau, with more than 40 years of R&D and manufacturing experience in semiconductor packaging, has published more than 520 peer-reviewed papers (375 are the principal investigator), 52 issued and pending US patents (36 are the principal inventor), and 23 textbooks (all are the first author), e.g., Chiplet Design and Heterogeneous integration Packaging (525 pages, Springer, 2023), and Flip Chip, Hybrid Bonding, Fan-In, and Fan-Out Technology (501 pages, Springer 2024). John is an elected IEEE Life-Fellow, IMAPS Life-Fellow, and ASME Fellow and has been actively participating in industry/academy/society meetings/conferences to contribute, learn, and share.

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EPTC2024 Professional Development Course #2

Photonic Technologies for Communication, Sensing, and Displays

Torsten Wipiejewski, Huawei Technologies

Course Objective:

This course will provide an overview on the various photonic technologies that enable optical communication, optical sensing, and modern display applications. These applications are key for the information and communication technology of today and path a way to the future. High speed optical communication from board level in data centers to long haul transmission requires photonic components with high speed and high reliability. We will discuss the main components such as laser diodes of various types, high speed optical modulators and photodetectors. We also address integration schemes such as photonic integrated circuits (PICs) and packaging aspects.

Photonic technologies are also widely used as sensors for various applications including health monitoring. One key advantage is the potential for non-invasive measurements that facilitates the usage by end-users without specific medical knowledge. Packaging should provide high accuracy solution at low cost.

Displays are the main media nowadays for bringing information to people. They range in size from smart watches to smart phones, laptops and tablets all the way to large screen TVs and video walls. We review current technologies and new developments such as quantum dots and micro LEDs with their specific packaging challenges. In particular, micro LEDs for large size displays require novel assembly technologies to mount chips of only several micro meter in size with extremely high yield at very low cost. The mass transfer of thousands of chips simultaneously is an option to achieve this challenging target.

Course Outline:

- Fundamental properties of photonic components
- Light sources (LEDs, laser diodes, others)
- Transmitter and receiver components in optical communication (lasers, modulators, photodetectors, passive optical components, photonic integrated circuits PICs, optical modules), monolithic and hybrid integration, packaging.
- Optical sensing elements and applications (spectrometers, light sources, lidar, photoacoustic sensors, frequency combs)
- Display technologies (liquid crystal displays LCD, organic light emitting diode OLED displays, quantum dot emissive layers, micro LED arrays and large size displays using chiplet mass transfer and bonding)
- Summary and outlook

Biography: Dr. Torsten Wipiejewski joined Huawei Technologies in 2014 and is responsible for the European technology sourcing of Huawei's Hardware Engineering Institute. His interest covers all hardware aspects for products ranging from smart watches to optical communication systems. He has also been appointed as Technical Advisor to the President of Huawei's European Research Institute. Previously, Torsten was an investor in renewable energy, CEO at Optogan (Germany, Finland) making blue LEDs, and COO at Firecomms (Ireland) making optical transceivers for automotive applications. He also held management positions at ASTRI

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in Hong Kong, Agility Communications in Santa Barbara, CA, USA as well as Infineon, Osram, and Siemens in Germany. Torsten received a “summa cum laude” Ph.D. degree in electrical engineering from the University of Ulm, Germany and has been an executive member of several international conferences. He was the General Chair of ECTC 2008 and has lectured several courses at conferences and universities. He holds more than 30 patents and has published over 100 scientific papers and presentations.

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EPTC2024 Professional Development Course #3

Wafer Bonding for Advanced Packaging Applications

Viorel DRAGOI, EVG

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- Die-to-wafer specific features compared to wafer-to-wafer bonding (samples preparation, alignment, etc.)
- Examples of die-to-wafer applications

8. Closing remarks

- Challenges for the future applications
- Metrology needs and future challenges

.**Biography:** Dr. Viorel DRAGOI graduated from the Faculty of Physics, University of Bucharest in 1995. He received his PhD from the Institute of Atomic Physics Bucharest, Romania, in 2000, with the topic “low temperature wafer bonding”.

After working in National Institute of Materials Physics, Bucharest for ten years first as a technician, later as junior scientist, he joined Max Planck of Microstructure Physics Halle (Saale), Germany, during the PhD.

He joined EV Group in 2001 as a wafer bonding technology process engineer and product manager for fusion wafer bonding equipment. His activities were focusing since then on process development based on wafer bonding with applications in MEMS and 3D integration. He is currently Chief Scientist for permanent wafer bonding and the manager of the Process Technology Development R&D team at EV Group headquarters in Austria. He is author and co-author of over 150 papers published in journals, proceedings volumes and book chapters.

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EPTC2024 Professional Development Course #4

Current and Future Challenges and Solutions in AI & HPC System and Thermal Management

Refai-Ahmed Gamal, AMD

Course Description:

Are you ready to dive into the forefront of AI and HPC system thermal management? This dynamic and interactive course, led by the renowned Dr. Gamal Refai Ahmed, is designed to equip you with cutting-edge knowledge and practical skills to tackle the current and future challenges in thermal management and packaging.

Dr. Refai Ahmed, a distinguished technical executive with over two decades of industry experience at giants like AMD, GE, and Cisco, brings unparalleled expertise to this course. His groundbreaking work in thermal management, silicon and power architecture, and advanced packaging technologies, supported by numerous patents and publications, sets the foundation for this comprehensive learning experience.

What You'll Learn:

1. **Thermal & Packaging Roadmap and Challenges (2020-2024)**
    - Gain insights from the latest IEEE publications by Refai-Ahmed et al.
    - Explore the Heterogeneous Integration Roadmap (HIR) and SRC roadmap MAPT.
2. **Next-Generation Thermal Management Architecture**
    - Understand the Seven Principles defining the next generation of thermal management architecture.
    - See practical examples of decoupling mechanical tolerances and coupling thermal management from a system level.
3. **First-Line and Second-Line Cooling Solutions**
    - Delve into the first line of silicon/package contact with the system via thermal interfaces.
    - Learn advanced approaches for extending system cooling limits.
4. **Advanced Cooling Techniques**
    - Discover the manufacturing, assembly, and reliability limitations of direct liquid cooling, immersion cooling, and microfluidic approaches.
    - Learn techniques to enable thermal loads beyond 1 kW.
5. **Dynamic Discussions and Hands-On Experience**
    - Engage in interactive discussions with industry peers.
    - Participate in practical, hands-on experiences that you can apply to your daily engineering practices.

Key Takeaways:

- A comprehensive understanding of current and future challenges in thermal management and packaging.
- Exposure to innovative solutions and state-of-the-art technologies.
- Practical insights that enhance daily engineering practices and drive industry advancements.

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Biography: Gamal Refai Ahmed, Ph.D., FIEEE, LFASEM, Fellow Canadiana Academy of Engineering, Fellow Engineering Insitute of Canada, AE, and a member of the National Academy of Engineering, is a distinguished technical executive renowned for his groundbreaking work in thermal management, silicon and power architecture, and advanced packaging technologies. With over two decades of experience at industry giants like AMD, GE, and Cisco, Dr. Refai-Ahmed has led high-impact projects, including pioneering new silicon and thermo-mechanical architectures for advanced technology nodes and enabling innovative packaging technologies for ASIC and embedded FPGA. His tenure at AMD as Senior Fellow and Chief Architect saw him spearheading thermal management solutions for Xilinx products and fostering research collaborations to expand HPC, NIC, AI, and ML ecosystems in data centers. He enhanced thermal management at GE for intelligent platform control systems and healthcare mobile systems, contributing significantly to GE's patent portfolio. Gamal has also defined technology directions and led projects that improved thermo-mechanical solutions for LED printing and UV LED products. Dr. Refai-Ahmed's academic background includes a Ph.D. in Mechanical Engineering from the University of Waterloo, Canada, with numerous publications and over 160 US and international granted and pending to his name, as well as more than 120 publications in IEEE, ASME, AIAA conferences and journals. His exemplary contributions have earned him prestigious accolades, including election to the National Academy of Engineering, IEEE Fellow, and the Presidential Medal from Binghamton State University. Actively involved in professional societies, Dr. Refai-Ahmed continues to influence the field through his roles in IEEE and ASME, shaping the future of high-performance computing and advanced packaging solutions.

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EPTC2024 Professional Development Course #5

Mechanics and Reliability of Lead-Free Solder Joints

Jeff Suhling, Auburn University

Abstract: This course will cover an overview of the experimental characterization and modeling approaches used for the mechanical behavior and reliability of lead-free solder materials used in electronics assembly and packaging. Emphasis will be placed on making the subject matter applicable by practicing semiconductor packaging engineers, and several example case studies will be incorporated from the automotive, aerospace, and computing industries. Topics to be covered include composition and microstructure of solders, methods used for mechanical characterization, experimental stress-strain and creep test data for lead free solders, material properties, constitutive models (elastic, plastic, creep, viscoplastic), mechanical response of single grain solder joints and associated modeling approaches, cyclic stress-strain behavior and fatigue laws, microstructural evolution and aging effects, thermal cycling reliability test data for various components, damage accumulation during cyclic loading, and finite element modeling methods for solder joint reliability. Several recent developments will be addressed including low temperature soldering and microbumps in advanced packaging. A detailed list of topics is presented in the outline below.

Course Outline:

1. Introduction to Solders Used in Electronic Packaging
    a. Composition and Microstructure
    b. Sn-Pb, SAC Alloys, SAC+X Alloys, Sn-Bi, Sn-Ag, etc.
    c. Low Temperature Solder (LTS) and SAC-LTS Mixed Solder Assemblies
2. Experimental Test Methods for Solder Mechanical Behavior
    a. Uniaxial and Shear Mechanical Testing (Stress-Strain, Creep)
    b. Nanoindentation Testing and Small Solder Joint Testing
3. Lead-Free Solder Mechanical Behavior (Bulk Solders)
    a. Uniaxial and Shear Stress-Strain Behaviors
        i. Literature Data for Important Lead-Free Solders
        ii. Material Properties (Modulus, Poisson's Ratio, Yield Stress, UTS)
        iii. Empirical Models, Temperature and Rate Dependencies
    b. Creep Behavior
        i. Literature Data for Important Lead-Free Solders
        ii. Material Properties (Creep Rate)
        iii. Empirical Creep Rate Models, Stress and Temperature Dependencies
    c. Constitutive Models
        i. Elastic, Elastic-Plastic, Creep, Viscoplastic (Anand)
        ii. Practical Application in Finite Element Codes and Industry Case Studies
4. Lead-Free Solder Mechanical Behavior (Single Grain Solders)
    a. Nanoindentation Data (Modulus, Hardness, Creep)
    b. Single Grain Mechanical Testing
    c. Anisotropic Behavior of Tin (Elastic, Plastic)
    d. Constitutive Modeling (Elastic, Crystal Plasticity)
    e. Case Studies and Practical Application to Advanced Packaging
5. Cyclic Stress-Strain Behavior
    a. Temperature and Strain Range Dependencies

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   b. Constitutive Modeling and Fatigue Laws
6. Effects of Aging and Damage
   a. Isothermal Aging Effects
      i. Microstructure Evolution
      ii. Stress-Strain and Creep Behaviors
      iii. Changes to Constitutive Models and Fatigue Laws
   b. Damage Due to Cyclic Loading
      i. Microstructure Evolution
      ii. Stress-Strain and Creep Behaviors (Bulk)
      iii. Changes to Constitutive Models and Fatigue Laws
7. Solder Joint Reliability
   a. Conventional Approaches Using Finite Element Analysis
      i. Constitutive Models (Anand, Creep Law)
      ii. FEM Meshing, Volume Averaging, Convergence
      iii. Failure Prediction
      iv. Case Studies from Industry
   b. Advanced Approaches Using Finite Element Analysis
      i. Evolving Microstructure and Damage Mechanics

Biography: Jeffrey C. Suhling received his Ph.D. degree in Engineering Mechanics in 1985 from the University of Wisconsin. He then joined the Department of Mechanical Engineering at Auburn University, where he currently holds the rank of Quina Distinguished Professor and Department Chair. From 2002-2008, he served as Center Director for the NSF Center for Advance Vehicle Electronics. His general research interests include solid mechanics, stress and strain analysis, material characterization, experimental mechanics, advanced and composite materials, finite element analysis and computational mechanics. He applies these areas to applications in electronic packaging, silicon sensors, and additive manufacturing. Dr. Suhling has authored or co-authored over 500 technical publications, and has an H-Index of 59 on Google Scholar. He has advised over 100 graduate students at Auburn University. He is a Fellow of ASME, and is a member of IEEE, SMTA, IMAPS, SEM, and TAPPI. He served as Chair of the Electrical and Electronic Packaging Division of ASME during 2002-2003, and was on the EPPD Executive Committee from 1998-2003. Dr. Suhling was the Technical Program Chair of the ASME InterPACK ‘07 Conference, and General Chair of the ASME InterPACK ‘09 Conference. He served as Vice President - Education for the IEEE Electronics Packaging Society from 2019-2022, and he currently serves as Vice President - Finance for the same organization. Suhling was the Program Chair of the 2018 IEEE ITherm Conference and General Chair of the 2019 IEEE ITherm Conference.

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EPTC2024 Professional Development Course #6

Failure Analysis of Advanced Packages: Fundamental, Skills, Philosophy and Case studies

Yong-Fen Hsieh, MA-Tek

Course Outline:

1.Overview of analytical skills and fundamental principle

1-1. Semiconductor Packaging Roadmap

1-2. Analysis Technology Roadmap

2. Current progress in tools and instrumentation

2-1. Failure analysis procedure, defined by AEC-Q004

2-2. Non-destructive Analysis, Level-1

- Time Domain Reflectometer (TDR)

2-3. Failure Analysis (FA), Level-2

2-4. Physical Failure Analysis (PFA) and Materials Analysis (MA), Level-3,4

- Cross-sectioning Polisher (CP) / Laser Cut, Plasma FIB, FIB
- Nanoprobing, I-V, EBIC, EBAC
- TEM Cs-TEM Ultra thin sample & AutoMeasurement
- Surface Analysis, SIMS, XPS, AES

2-5. Reliability Testing

- Board Level RA Service
- Shadow Moiré Measurement System

3. Case Demonstration - Some Examples of Integrated Service Cases

COWOS issues, UBM layer crack after TCT, Stealth dicing induce WLCSP, Chip sidewall crack, Solder ball open, Bump open, Bonding wire short, Particle issue induced short failure, Assembly & SMT failure, Assembly Issue, TEM TSV, TGV.

Biography:

Dr. Hsieh, Chairman and CEO / Materials Analysis Technology Inc., received her BS, MS, and Ph.D degree of Materials Science and Engineering from National Tsing-Hua University in Taiwan in 1981, 1983, and 1988 respectively. Her major interest of academic research was mainly focused on the metal contact formation on semiconductors.

Dr. Hsieh extended her professional interests to versatile materials systems when doing her postdoctoral research in AT&T Bell Labs. Murray Hill, NJ. During the time (1989-1991), she had been working with

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many research groups and published many papers on Cobalt implanted silicide formation, AlGaAs/GaAs surface emitting lasers, GaSb/InSb/GaSb laser diode, Si-Ge heterojunction bipolar transistors, YBCO/$LaAlO_3$ superconductors, and $FeSi_3$/GaAs metal contact formation. She also partially supported the physical analysis of the process development team of 4Mb SRAM at Allentown, PA, which upgraded her skills, not only in the fundamental studies, but also in the technology development of IC devices and products.

Dr. Hsieh joined the Taiwanese government sponsored research organization, ITRI, after finishing the academic researches. She was associated with MRL, working on the AlGaAs Super-high Brightness LED project and with ERSO as integration engineer of BiCMOS and 16Mb DRAM projects. It elucidated her ability to conduct an up-to-date industrial TD project from a scientific perspective.

Dr. Hsieh commenced her career in industry since 1994. She was associated with UMC, IC Wafer Foundry, as the department heads of Materials Analysis, Failure Analysis, and Quality Assurance in QRA division. After a inter-group companies transfer, she was heading the Quality Management Division of Unipac Optoelectronic Corp., the first TFT-LCD Manufacturer in Taiwan, in 2000-2001 and in charge of the operation of LCOS(Liquid Crystal on Si) Business Division after the merge of AU Optronics (ADT and Unipac).

With the wide knowledge base in research, integration, FA, and QRA in various industries, Dr. Hsieh decided to make every endeavor to contribute the community by running an analytical lab, MA-tek., in Aug. 2002. It owns 16 labs in HsinChu, JuBei, Tainan/Taiwan, Shanghai, Xiamen, ShenZhen, SuZhou/China, and Nagoya, Kumamoto, Hokkaido/Japan now and is known to be the first tier materials analysis lab worldwide. In 2006, it was elected to be the fast growth company in top 50/Taiwan and top 500/Asia by Delloitte. In 2008, it was the ONLY service lab awarded as the industrial excellence by Economy ministry of Taiwan. It is also formally listed in Taiwan stock market (No.3587) on Aug.18, 2009.

Her major achievement covers the following items:

- ***Distinguished Alumni of NTHU, Taiwan***, 台灣清華大學 傑出校友, **2009**
- ***Chairman, Taiwan NTHU Alumni Association***, 台灣清華大學 校友會理事長, **2015-2018**
- ***Featured in "Women in Technology" EE Times***, 獲選電子工程專輯 全球 20 位傑出女性執行長 工程技術職類別, **2017**
- ***Fellow, Taiwan Materials Science Society***, 台灣材料學會 會士, **2018**
- ***EY Entrepreneur Award***, 安永企業家 尖端服務獎, **2018**
- ***ERSO Award***, 潘文淵文教基金會, **2021**
- ***The Best Female CEOs in Taiwan by Harvard Business Review***, 獲選《哈佛商業評論》台灣最佳女性 CEO, **2021 and 2023**
- ***200 Best Under a Billion, Forbes Asia 2024***