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Foreword Message

On behalf of the Organizing Committee and Technical Committee, it is our pleasure to welcome you to the 20th Electronics Packaging Technology Conference (EPTC), held at Asia's leading leisure destination Resort World Sentosa, Singapore, from December 4th – 7th 2018. This premier international conference is organized by the IEEE RS/EPS/EDS Joint Singapore Chapter and co-sponsored by the IEEE Electronic Packaging Society (EPS), with the aim of bringing together engineers and researchers from the global microelectronics packaging community, such as semiconductor companies, foundry and OSAT service providers, equipment manufacturers, materials suppliers, research institutions and universities, under one roof for knowledge sharing and networking.

At the 20th EPTC, over 190 technical papers and 20 invited presentations are scheduled to be presented in 35 oral sessions and two interactive presentation sessions. The oral sessions will feature selected papers on key topics such as Advanced Packaging, TSV/Wafer Level Packaging, Interconnection Technologies, Emerging Technologies, Materials and Processing, Equipment and Process Automation, Electrical Simulations & Characterization, Mechanical Modeling & Simulations, Thermal Characterization & Cooling Solutions, Quality, and Reliability & Failure Analysis. Authors from over 24 countries and various industries, research institutes and universities are expected to present their work at the 20th EPTC, making it a truly global packaging conference.

As EPTC is celebrating its 20th anniversary, an extra day of special programs on December 5th featuring three keynote talks and two special panel sessions will be added to the usual conference program. The conference opening Keynotes will be deliberating on "Visualizing the Packaging Roadmap" by Mr Ivor Barber, Corporate VP for Packaging at AMD; "Thermal Packaging of High Flux Power and Logic Components – History and Recent Progress" by Dr Avram Bar-Cohen, Principal Engineering Fellow at Raytheon Corporation; and "Packaging and Heterogeneous Integration by Ms Jean Trewhella, Director of Packaging Research and Development at Globalfoundries. On Wednesday, December 5th at 1.30pm, Dr. Bill Chen, ASE Fellow and Senior Technical Advisor will chair the panel session on "Heterogeneous Packaging" with four distinguished panel speakers including Dr. Gamal Refai-Ahmed (Xilinx, ASME), Mr. Mike Delaus (Analog Devices), Dr. Yu-Po Wang (SPIL) and Mr. Manish Ranjan (Lam Research). On the same day at 4.00pm, Dr. Yoon Seung Wook, Business Development Director at JCET StatsChipPac will chair the panel session on "Packaging for next generation automobiles/ autonomous cars" with four more distinguished panel speakers including Mr. Gaurab Majumdar (Mitsubishi Electric), Ms. LC Tan (NXP Semiconductors), Mr. Christophe Bouquet (Infineon Technologies) and Mr. Santosh Kumar (Yole Développement).

In addition to the technical sessions on December 6th and 7th, a closing panel session on "Next Generation Packaging Technologies" will be moderated by Mr Shigenori Aoki, Fujitsu Laboratories with four distinguished panel speakers including Dr Yasumitsu Orii (NAGASE), Mr Yasushi Masuda (Fujitsu Advanced Technologies), Dr Hideyuki Nasu (Furukawa Electric) and Dr Toshihisa Nonaka (Hitachi Chemical) on December 7th.

EPTC also offers six professional development courses (PDC) on Tuesday, December 4, by experts from both industry and academia. It is an opportunity for the participants to learn new technologies and broaden their knowledge base. In addition, there will be an exhibition corner and exhibitors' presentations from leading semiconductor companies showcasing their latest technologies and products. Exhibitions will be on December 5th, 6th and 7th. EPTC will also provide great opportunity to network and discuss technical and business matters.

We would like to take this opportunity to thank all our sponsors, exhibitors, authors, speakers, PDC instructors, session chairs, committee members, EPTC Board members, EPS BoG members, conference secretary, website support team, media partners, partnering associations, conference partners, souvenir sponsors, publicity team, suppliers and vendors as well as all the conference associates and volunteers for their support and hard work. We also thank all conference delegates for making this event a great success. We hope that the 20th Electronics Packaging Technology Conference (EPTC 2018) in vibrant Singapore is an informative and memorable event, and we are grateful for your feedback.

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Intro-duction to EPTC

The Electronics Packaging Technology Conference (EPTC 2018) is an International event organized by the IEEE Reliability/CPMT/ED Singapore Chapter and sponsored by IEEE CPMT Society. CPMT has recently been renamed as EPS (Electronics Packaging Society). This year we celebrate 2 decades of excellence and comradeship built through the EPTC. Special programmes would be arranged, follow us on this webpage!

EPTC 2018 will feature technical sessions, short courses/ forums, an exhibition, social and networking activities. It aims to provide a good coverage of technological developments in all areas of electronic packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.

Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in Asia and is well attended by experts in all aspects related to packaging technology from all over the world. EPTC is the leading flagship conference of EPS Society in Region 10.

Conference Topic

Advanced Packaging : Advanced flip-chip, 2.5D & 3D, PoP, embedded passives & actives on substrates, System in Package, embedded chip packaging technologies, panel level packaging, RF, Microwave & Millimeter-wave, power and Rugged Electronics Packaging etc.

TSV/Wafer Level Packaging : Wafer level packaging (Fan In/Fan Out), embedded chip packaging, 2.5D/3D integration, TSV, silicon & glass interposers, RDL, bumping technologies, etc.

Interconnection Technologies : Au/Ag/Cu/Al wire-bond / wedge bond technology, flip-chip & Cu pillar, solder alternatives (ICP, ACP, ACF, NCP, ICA), Cu to Cu, wafer level bonding & die attachment (Pb-free) etc.

Emerging Technologies : Packaging technologies for MEMS, biomedical, optoelectronics, internet of things, photovoltaic, printed electronics, wearable electronics, photonics, LED, etc.

Materials & Processes : Advanced materials, 3D materials, photoresists, polymer dielectrics, solder materials, die attach, underfill, substrates, leadframes, PCB etc for advanced packaging, and assembly processes using advanced materials, etc.

Equipment and Process Automation : New processes development, equipment automation, equipment hardware development/improvements, data analytics, in-situ metrology, etc.

Electrical Simulations & Characterization : Power plane modeling, signal integrity analysis of package. 2D/2.5D/3D package level high-speed signal design, characterization and test methodologies, etc.

Mechanical Modeling & Simulations : Thermo-mechanical, moisture, fracture, fatigue, vibration, shock and drop impact modeling, chip-package interaction, reliability, virtual prototyping, etc.

Thermal Characterization & Cooling Solutions : Thermal modeling and simulation, component, system and product level thermal management and characterization.

Quality, Reliability & Failure Analysis : Component, board, system and product level reliability assessment, interfacial adhesion, accelerated testing, failure characterization, etc.

Conference Program

* All events are held at the Resorts World Sentosa (RWS), Singapore, unless otherwise stated.

* This Conference Program is subjected to changes (confirmation of the breakout sessions is subjected to the authors' registration and payment)

TUESDAY, 4TH DECEMBER 2018

07:30am - 08:30am	Registration	Leo 1's Foyer
	Professional Development Courses	
08:30am - 12:00pm	**01: Introduction to Fan-out Wafer Level Packaging** - Dr. Beth Keser	Virgo 1
	02: Advanced Integrated Circuit Design for Reliability - Dr. Richard Rao	Virgo 2
	03: 3D SIP For ASIC and DRAM Integration - Dr. Li Li	Virgo 3
12:00pm - 01:30pm	Lunch	Gemini 1-2
01:30pm - 05:00pm	**04: Understanding Flip Chip Technology and Its Applications** - Mr. Eric Perfecto	Virgo 1
	05: Introduction to 3D Interconnect and Packaging Technologies - Prof. Sarah Kim	Virgo 2
	06: Power Electronic Packaging Reliability, Materials, Assembly and Simulation - Dr. Ning-Cheng Lee / Dr. Yong Liu / Prof. Sheng Liu	Virgo 3

WEDNESDAY, 5TH DECEMBER 2018

08:00am - 08:45am	Registeration	Leo 1's Foyer
08:45am - 09:30am	Opening Ceremony	Leo 1-4
09:30am - 10:15pm	**Keynote 01: Visualizing the Packaging Roadmap** - by Mr. Ivor Barber	
10:15am - 10:45am	Tea/Coffee Breaks-01:	Pisces
10:45am - 11:30am	**Keynote 2: Thermal Packaging of High Flux Power and Logic Components – History and Recent Progress** - Dr Avram Bar-Cohen	Leo 1-4
11:30am - 12:15pm	**Keynote 3: Packaging and Heterogeneous Integration** - Ms Jean Trewhella	
12:15pm - 01:30pm	EPS Luncheon	Virgo
01:30pm - 03:30pm	**Plenary Session 1: Heterogeneous Packaging -** Dr. William Chen (Moderator) Dr. Gamal Refai-Ahmed | Mr. Mike Delaus | Mr. Manish Ranjan | Dr. Yu-Po Wang	Leo 1-4
03:30pm - 04:00pm	Tea/Coffee Breaks-02:	Pisces
04:00pm - 06:00pm	**Plenary Session 2: Packaging for next generation automobiles/autonomous Vechicles -** Dr. Seung Wook Yoon (Moderator) Dr. Gourab Majumdar | Ms. LC Tan | Mr. Christophe Bouquet | Mr. Santosh Kumar	Leo 1-4

THURSDAY, 6TH DECEMBER 2018

08:30am - 09:00am	**Invited Presentations**	
	01: Packaging for Performance Scaling - Mr. Sam Karikalan	Gemini 2
	02: Three-Dimensional Embedded Capacitor in Through-Silicon Via (TSV) - Prof. Tan Chuan Seng	Leo 1
	03: Soldering Material Challenges For Heterogeneous Integration and Assembly - Ms. Lim Sze Pei	Leo 2
	04: Emerging NAND Memory Packaging Challenges - Dr. Gokul Kumar	Leo 3
	05: Microfluidic Electroless Interconnection Process for Low-Temperature, Pressureless Chip-stacking - Prof. Robert Kao	Leo 4
09.00am - 10.00am	**Technical Session A (5 tracks)**	
	S-01: Advanced Packaging I	Gemini 2
	S-02: Interconnect Technologies I	Leo 1
	S-03: Materials and Processing I	Leo 2
	S-04: Emerging Technologies I	Leo 3
	S-05: Thermal Characterization & Cooling Solutions I	Leo 4
10:00am - 11:00am	Tea/Coffee Breaks-03: **Interactive Session I and Exhibitor Presentation 1**	Pisces
11.00am - 12.20pm	**Technical Session B (5 tracks)**	
	S-06: Advanced Packaging II	Gemini 2
	S-07: Quality, Reliability & Failure Analysis I	Leo 1
	S-08: Materials and Processing II	Leo 2
	S-09: Electrical Simulation & Characterization I	Leo 3
	S-10: Mechanical Simulation & Characterization I	Leo 4
12:20pm - 01:50pm	Lunch: **Best paper Award, EPTC 2018 committee Appreciation**	Virgo

THURSDAY, 6TH DECEMBER 2018

01:50pm - 02:20pm	**Invited Presentations**	
	06: Submicron Polymer Re-distribution Layer Technology for Advanced InFO Packaging - Dr. Han-Ping Pu	Gemini 2
	07: A Framework for Reliability Assessment of Chemical-Induced Display Delamination - Dr. Kedar Hardikar	Leo 1
	08: Temporary Wafer Bonding Technology for Advanced Packaging - Dr. Dongshun Bai	Leo 2
	09: Technology Trends for Large Area Panel Level Packaging - Dr. Tanja Braun	Leo 3
	10: ESD, EOS and AMR - Dr. Stevan Hunter	Leo 4
02:20pm - 03:40pm	**Technical Session C (5 tracks)**	
	S-11: TSV & WLB Packaging I	Gemini 2
	S-12: Quality, Reliability & Failure Analysis II	Leo 1
	S-13: Materials and Processing III	Leo 2
	S-14: Emerging Technologies II	Leo 3
	S-15: Electrical Simulation & Characterization II	Leo 4
03:40pm - 04:40pm	Tea/Coffee Breaks-04: **Interactive Session 1 and Exhibitor Presentation 2**	Pisces
04:40pm - 06:00pm	**Technical Session D (5 tracks)**	
	S-16: Thermal Characterization & Cooling Solutions II	
	S-17: Interconnect Technologies II	Leo 1
	S-18: Materials and Processing IV	Leo 2
	S-19: Emerging Technologies III	Leo 3
	S-20: Mechanical Simulation & Characterization II	Leo 4
01:50pm - 06:00pm	**Heterogeneous Integration Roadmap Workshop** (Parallel Session to Technical paper tracks)	Gemini 1
06:30pm - 09:30pm	**Conference Banquet**	

FRIDAY, 7TH DECEMBER 2018

08:30am - 09:00am	**Invited Presentations**	
	11: TSV interconnect based 3D/2.5D IC packaging technology and market trends - Mr. Santosh Kumar	Gemini 2
	12: Engineering Green Electronics - Prof. David Mark Harvey	Leo 1
	13: Organic substrate material with low transmission loss and effective in suppressing package warpage for 5G application - Mr. Shunsuke Tonouchi	Leo 2
	14: Electronic Materials and Packaging Trends in the Era of Digital Transformation - Ms.Rozalia Beica	Leo 3
	15: Thermal and Failure Analysis of Advanced Sub-Micron Devices Using Transient Thermoreflectance Thermography - Prof. Andrew Tay	Leo 4
09.00am - 10.20am	**Technical Session E (5 tracks)**	
	S-21: TSV & WLB Packaging II	Gemini 2
	S-22: Interconnect Technologies III	Leo 1
	S-23: Materials and Processing V	Leo 2
	S-24: Emerging Technologies IV	Leo 3
	S-25: Thermal Characterization & Cooling Solutions III	Leo 4
10:20am - 11:10am	Tea/Coffee Breaks-05: **Interactive Session 2 / Exhibitor Presentation 3**	Pisces
11.00am - 12.30pm	**Technical Session F (5 tracks)**	
	S-26: Advanced Packaging III	Gemini 2
	S-27: Equipment and Process Automation	Leo 1
	S-28: Materials and Processing VI	Leo 2
	S-29: Electrical Simulation & Characterization III	Leo 3
	S-30: Mechanical Simulation & Characterization III	Leo 4
12:30pm - 01:30pm	Lunch: **EPTC 2019 Introduction; Sponsors appreciation**	Virgo

FRIDAY, 7TH DECEMBER 2018

01:30pm - 02:00pm	**Invited Presentations**	
	16: Novel Thin Wafer De-bonding System for 3D TSV Multi-Chip Packaging of High Bandwidth Memory Devices - Dr. Minwoo Daniel Rhee	Gemini 2
	17: Low temperature interconnect technology using Sn-Bi alloy system for high performance packages - Mr. Kei Murayama	Leo 1
	18: Effects of Aging on the Reliability of Electronic Products Incorporating Lead Free Solders - Prof. Jeff Suhling	Leo 2
	19: Package Level Systems Integration: A key to maintaining the pace of progress - Dr. Bill Bottoms	Leo 3
	20: LED multiphysics modelling for "Industry 4.0", an approach proposed by the Delphi4LED European project - Prof. Marta Rencz	Leo 4
02:00pm - 03:20pm	**Technical Session G (5 tracks)**	
	S-31: TSV & WLB Packaging III	Gemini 2
	S-32: Interconnect Tenhnologies IV	Leo 1
	S-33: Quality, Reliability & Failure Analysis III	Leo 2
	S-34: Emerging Technologies V	Leo 3
	S-35: Thermal Simulation and Modeling IV	Leo 4
03:20pm - 03:40pm	Tea/Coffee Breaks-06: **Interactive Session 2**	Pisces
03:40pm - 05:40pm	**Plenary Session 3: Next Generation Packaging Technologies** **-** Mr. Shigenori Aoki (Moderator) Dr. Yasumitsu Orii | Mr. Yasushi Masuda | Dr. Hideyuki Nasu | Dr. Toshihisa Nonaka	Virgo
05:40pm - 06:00pm	**Closing Ceremony: Lucky Draw**	Virgo

Keynote Talk 1

Visualizing the Packaging Roadmap

Wednesday, 5th December
<09:30am - 10:15am>
Leo 1-2-3-4

BY

MR. **IVOR BARBER**
Vice President,
Packaging Engineering, AMD

Roadmaps such as Moore's Law and the ITRS roadmap have guided SOC scaling for decades as the Economic and Technological driving force behind the advancement of the Semiconductor Industry.

Packaging solutions have generally followed these indicators by accommodating the predicted die size, IO, power and electrical performance requirements.

With the end of Moore's Law as an economic driver at 28nm and publication of the final edition of the ITRS in July 2016 we find Packaging is now on the center stage of semiconductor innovation - but what roadmap do we follow?

The presentation will discuss prior roadmaps and how the packaging industry is responding with a product based integrated solution roadmap – the HIR or Heterogenous Integration Roadmap. The presenter will discuss the goals of Heterogenous Integration and the package solutions this will drive.

IVOR BARBER is currently Corporate VP for Packaging at AMD with responsibility for all Packaging activity from Design through High Volume Manufacturing.

With over 35 years experience in the Semiconductor Industry Ivor has held various Engineering and Management positions in Assembly, Package Characterization and Package Design at National Semiconductor, Fairchild Semiconductor, VLSI Technology, LSI Corporation and Xilinx.

Ivor graduated from Napier University in Edinburgh, Scotland in with a Bachelors degree in Technology and holds 15 US patents related to packaging.

Keynote Talk 2

Thermal Packaging of High Flux Power and Logic Components- History and Recent Progress

Wednesday, 5th December
<10:45am - 11:30am>
Leo 1-2-3-4

DR. AVRAM BAR-COHEN
Principal Engineering Fellow
Raytheon – Space and Airborne Systems
Rosslyn, Va

Near-junction thermal barriers severely limit the electronic performance of high-speed, high heat flux microelectronic devices. While thermal packaging technology has been a key enabler in the development of today's nano-scale high performance, high reliability microelectronic systems, a new thermal management paradigm – embedded cooling – is needed if we are to overcome the triple threat of high-power, "hotspots," and 3D integration in applications as diverse as high performance computing, power electronics, and RF systems. Recent "embedded cooling" efforts, focused on the use of diamond substrates and on-chip microfluidics, have demonstrated the efficacy of suppressing "hot spots" dissipating more than 30kW/cm2 and successfully cooling chips with 1 kW/cm2 power dissipation. These efforts will be presented and discussed.

DR. AVRAM BAR-COHEN is an internationally recognized leader in thermal management of microelectronics, the IEEE Electronic Packaging Society President for 2018-2019 and Life Fellow of IEEE, as well as Honorary Member of ASME, and is currently serving as a Principal Engineering Fellow at Raytheon Corporation – Space and Airborne Systems. His publications, lectures, short courses, and research, as well as his US government and Professional service in IEEE and ASME, have helped to create the scientific foundation for the thermal management of electronic components and systems. His current efforts focus on embedded cooling, including two-phase microchannel coolers, on-chip thermoelectrics, and diamond substrates for high heat flux electronic and photonic components in computational, radar, and directed energy systems.

Bar-Cohen is a former Editor-in-Chief of the IEEE CPMT Transactions and has represented the Society as a Distinguished Lecturer for more than 15 years. He recently completed his service as a Program Manager in the Microsystem Technology Office at the Defense Advanced Projects Agency in Virginia and had earlier served as Department Chair of Mechanical Engineering and Distinguished University Professor at the University of Maryland – College Park.

In 2014 Bar-Cohen was honored by the IEEE with the prestigious CPMT Field Award and had earlier been recognized with the CPMT Society's Outstanding Sustained Technical Contributions Award (2002). Among other awards, Bar-Cohen received the Luikov Medal from the International Center for Heat and Mass Transfer in Turkey (2008) and ASME's Heat Transfer Memorial Award (1999), Edwin F. Church Medal (1994), and Worcester Reed Warner Medal (1990).

In addition to serving as the Editor-in-Chief of WSPC's Encyclopedia of Thermal Packaging and the co-editor of the Advanced Integration and Packaging book series, Bar-Cohen has co-authored Dielectric Liquid Cooling of Immersed Components (WSPC, 2013), Design and Analysis of Heat Sinks (Wiley, 1995), and Thermal Analysis and Control of Electronic Equipment (McGraw-Hill, 1983), and has edited/co-edited 28 other books in this field. He has authored/co-authored more than 400 journal papers, refereed proceedings papers, and chapters in books and has delivered some 100 keynote, plenary and invited lectures at major Conferences, Symposia, and college campuses throughout the world.

Keynote Talk 3

Packaging and Heterogeneous Integration

Wednesday, 5th December
<11:30am - 12:15pm>

Leo 1-2-3-4

MS. JEAN TREWALLA
Director, Packaging Research and Development,
GLOBALFOUNDRIES

Advances in Moore's law are slowing due to cost of design and fabrication in advanced nodes. In addition, packaging has not scaled with Moore's Law. Package scaling now must happen to bring higher performance solutions to market required for AI, ML, and GPU applications. Most solutions require heterogeneous integration of chips from different nodes and processes. Integration of processors with memory in 2.5D has been the first driver for heterogeneous integration but have not been without challenges. 3D and SiPh technologies are next. 3D SRAM stacks on logic will enable an order of magnitude leap in interconnect density and power reduction per interconnect. Further package scaling enabling heterogeneous integration will be needed for system level solutions. Application needs, challenges, and solutions will be discussed.

JEAN M. TREWHELLA received her B.S. in Physics from Antioch College (1987) and her M.S. in Applied Physics from Columbia University (1992). She joined the T.J. Watson Research Center, IBM, in 1988 where her work included polymer optical waveguides fabrication, electrical modeling, and opto-mechanical package design for data communication systems. In 2000 she created the High Speed Electrical and Optical Packaging Group in IBM Research directing work in electrical link signal integrity, advanced 1st and 2nd level packaging, and low cost high speed opto-mechanical packaging. She received an Outstanding Technical Achievement Award for her work on 10Gbps Ethernet Transceiver Development in 2003. In 2005 she drove IBM wide team of engineers and scientists to highlight key disruptive technologies synthesizing the messages into three GTO topics: Technology, Application-Optimized Systems, and Services 2.0. From 2006-2008 she was responsible for the Electronic Packaging Integration Group in IBM STG where her team developed the power5 and z10 system hardware. Currently Jean Trewhella is the Director of IBM Packaging Research and Development Center with responsibility of 3D, low cost, and high performance packaging technology for current and future products.

Ms. Trewhella was on the Strategic Advisory Board for NSF STC - Materials & Devices for Information Technology Research 2004-2008, she served as the General Chair of the 60th ECTC and is currently a member at large of the CPMT Board of Governors. She has authored numerous papers and holds over 20 US patents.

Panel Session 1
Heterogenous Integration

Wednesday, 5th December
<13:30 - 15:30pm>
Leo 1-2-3-4

MODERATED BY
DR. **WILLIAM CHEN (BILL)**
ASE Fellow & Senior Technical Advisor, ASE Group

WILLIAM CHEN (BILL) holds the position of ASE Fellow & Senior Technical Advisor at ASE Group. Prior to joining the ASE, he was Director at the Institute of Materials Research & Engineering (IMRE) in Singapore, following a distinguished career at IBM Corporation. Bill is a past President of the IEEE Electronics Packaging Society, and has been elected a Fellow of IEEE and a Fellow of ASME. In 2018, he received the IEEE Electronics Packaging Field Award, recognizing his contribution to electronic packaging, from research & development through industrialization. Bill currently chairs the Heterogeneous Integration Roadmap initiative.

DR. **GAMAL REFAI-AHMED**
Fellow Canadian Academy
of Engineering, Xilinx inc.

DR. GAMAL REFAI-ADMED is a Distinguished Engineer (and Adjunct Professor in Watson School of Engineering and Applied Science SUNY Binghamton. He obtained the M. A. SC. and Ph. D. degrees in Mechanical Engineering from the University of Waterloo.

Dr. Refai has made important contributions to the electronics packaging. He has significantly advanced this scientific field through his development of ground-breaking electronics cooling technologies.

His engineering practice has not only impacted the academic community, but has also greatly influenced the consumer electronics, telecommunications and energy industries. Due to his pivotal discoveries, many types of electronic systems are able to maintain a higher performance even among the most challenging circumstances. His inventions have also led to improved performance, versatile, reliable, and commercially viable electronic systems for a wide variety of product offerings. He is the author of more than 90 technical papers and more than 100 US patents/ International Patents/ Pending patents.

Dr. Refai is an Associate Editor of Journal Components and Packaging, IEEE and Journal of thermal Sciences and Engineering and Applications, Transactions of the ASME. Gamal is the recipient of 2008 excellent thermal management award, 2010 best Associate Editor J Electronics Packaging, 2010 Calvin Lecture and 2013 K16- Clock award in recognition for his scientific contributions and leadership of promoting best electronics packaging engineering practice. In 2014, Gamal received the IEEE Canada R. H. Tanner Industry Leadership for sustained leadership in product development and industrial innovation. In 2015, the ASME service award and the 2016 IEEC SUNY Binghamton Innovation leader of the year.

MR. **MIKE DELAUS**

Wafer-Level Package Development Group at ADI.

MIKE DELAUS received his B.S. degree in Materials Science Engineering from MIT in 1982. He joined the Advanced Process Development Group at Analog Devices as a front-end process development engineer in 1988. Since 2006, he has directed ADI's wafer-level package development activities, responsible for wafer-level bumping, flip-chip and fanout packaging. He also manages development programs involving Through-Silicon Vias (TSVs), 3D integration and other advanced packaging technologies.

MR. **MANISH RANJAN**

Managing Director, Advanced Packaging Customer Operations, LAM Research

MANISH RANJAN is the Managing Director for Advanced Packaging Customer Operations at Lam Research. He joined Lam in 2015 and is currently responsible for managing marketing, business development and business operations activities for various deposition, etch and clean products in advanced packaging market segment.v

Prior to joining Lam, Manish was the Head of Advanced Packaging and Nanotechnology segment at Ultratech Inc where he was responsible for managing all aspects of product, business and market development for lithography market segment. During his tenure at Ultratech, he led profitable market share growth to establish a dominant market share for the lithography product portfolio. He also worked at Lucent Technologies as the Product Technology Manager in the Analog Product Business Unit where he managed technical and business issues related to flip chip and WLP technology development. Manish has received a Master of Science degree in Industrial Engineering from State University of New York at Binghamton. He has also received a Master of Business Administration from The Wharton School of Business in Philadelphia.

DR. **YU-PO WANG**

Senior Director, CRD Center, SPIL

Education:
Ph.d., Mechanical Engineering, State University Of New York At Binghamton, New York, U.S.A.

Experience:
1997-1998 Gintic Institute Of Manufacturing Technology, Singapore
1998-Present Spil, Taiwan

Panel Session 2
Packaging for next generation automobiles/ autonomous Vehicles

Wednesday, 5th December
<4:00pm - 6:00pm>
Leo 1-2-3-4

MODERATED BY

DR. SEUNG WOOK YOON

Director / Group Technology Strategy
Company: STATS ChipPAC Pte Ltd. JCET Group

DR. YOON is currently working as director of Wafer Level Products in Group Technology Strategy, JCET Group. His major interests are for Advanced Wafer Level Packaging and Wafer Level Integration Technology including eWLB/Fan-out/Fan-in WLP, SiP, TSV, IPD and integrated 3D IC packaging.

Prior to joining STATS CHIPPAC LTD, He was deputy lab director of MMC (Microsystem, Module and Components) lab, IME (Institute of Microelectronics), A*STAR, Singapore. "YOON" received Ph.D degree in Materials Science and Engineering from KAIST, Korea. He also holds MBA degree from Nanyang Business School, Singapore. He has over 300 journal papers, conference papers and trade journal papers, and over 20 US patents on microelectronic materials and electronic packaging. Currently working as technical committee member of various international packaging technology conferences, EPTC, ESTC, iMAPS, IWLPC and SEMI.

DR. GOURAB MAJUMDAR

Senior Fellow,Semiconductor & Device Group,
Mitsubishi Electric Corporation, Japan

GOURAB MAJUMDAR (b. 1955) received Bachelor of Technology degree in electrical engineering from Indian Institute of Technology (IIT), Delhi, India in 1977 and Doctor of Engineering degree from Kyshu Institute of Technology (KIT), Japan in 2005. He lived in Japan since September, 1978 and started his career in the country at Mitsubishi Electric Corporation on a special OJT program. He was employed by the company in 1980 and, since 1983, has worked in its units responsible for advanced power semiconductor development, design and applications. From April-2012 to March-2017, he served as Executive Fellow, Semiconductor & Device Group of Mitsubishi Electric Corporation. On April-2017, he was reemployed by Mitsubishi Electric, Japan and currently acting as Senior Fellow, Semiconductor & Device Group of the same company. He has published and co-authored many technical papers and books on power devices and holds several patents in the related fields. He is a recipient of the prestigious National Invention Award in Japan in 2005 for invention of the IPM (Intelligent Power Module) fundamental concept and has also received a number of other prestigious awards, including the "Monozukuri Nihon Taishou" (Japan Craftsmanship Grand Prix) award from the honorary Minister of Economy, Trade and Industry in 2013 for contribution in development and commercialization of various generations of IPM devices. He served as the General Chairman of ISPSD 2013 and has been participating as a member of both PCIM's Advisory Board and ISPSD's Advisory Committee. He received IEEE-ISPSD Contributory Award in 2017 for playing and active role in the field of Intelligent Power Module and Power ICs and contributing largely to the ISPSD. He was nominated to be one of the first 32 inductees to IEEE-ISPSD Hall Of Fame for his pioneering global role in progressing IGBT and IPM technologies, and was inducted to the same in May 2018.He has been a visiting lecturer of advanced power semiconductor devices at both Kyushu University and Tokyo Institute of Technology (TIT) for several years till date. Also, he has been bestowed with Honorary Professorship in 2016 by Amity University, India.

MS. LC TAN
Senior Director, Assembly Process Innovation at NXP Semiconductors

LC TAN is currently Senior Director, Assembly Process Innovation at NXP Semiconductors . She leads packaging and process technologies development supporting new product introductions for the corporation . LC holds 28 issued patents and holds a Master of Science degree in semiconductor packaging as well as MBA degree .telectronics and communications from E.S.I.E.E Paris (France), Karlsruhe (Germany) and Essex (U.K.).

MR. CHRISTOPHE BOUQUET
Infineon Singapore

CHRISTOPHE BOUQUET has been working in Infineon Singapore since 2000. Starting as an IC design & verification engineer, he moved on to multiple roles including project and program management within the automotive microcontroller business line. He was there responsible for several microcontroller products, including the first automotive qualified 130nm embedded flash device. He had the opportunity to work in different fields, including software and application engineering. Since 2015, Christophe shifted his focus to packages for Automotive and is now leading the automotive package concept group in Infineon Singapore.

Christophe is located in Singapore, where he has been living since 1992. He holds a joint Master degree in electronics and communications from E.S.I.E.E Paris (France), Karlsruhe (Germany) and Essex (U.K.)

MR. SANTOSH KUMAR
Director & Principal Analyst
Yole Développement

SANTOSH KUMAR is currently working as Director & Principal Analyst at Yole Développement. He is involved in the market, technology and strategic analysis of the microelectronic assembly and packaging technologies. His main interest areas are advanced IC packaging technology including equipment & materials. He is the author of several reports on fan-out / fan-in WLP, flip chip, and 3D/2.5D packaging.

He received the bachelor and master degree in engineering from the Indian Institute of Technology (IIT), Roorkee and University of Seoul respectively. He has published more than 40 papers in peer reviewed journals and has obtained 2 patents. He has presented and given talks at numerous conferences and technical symposiums related to advanced microelectronics packaging.

Panel Session 3
Next Generation Packaging Technologies

Friday, 7th December
<03:40pm - 05:40pm>
Virgo 1-4

MODERATED BY
MR. **SHIGENORI AOKI**
Fujitsu Laboratories

SHIGENORI AOKI received the B.S. degree from Kyoto University, Kyoto, Japan in 1985 in Physics.

In 1985, he joined Fujitsu Laboratories Ltd., Kawasaki, Japan. He has successively worked for high density packaging technologies and materials, including multi-layer ceramic substrate for mainframes,millimeter wave packaging for automotive radars, parallel-optical packaging for interconnects, and liquid cooling for supercomputers.enori Aoki

Mr. Aoki is the current Vice Chair of the IEEE EPS Japan Chapter, and a Member of the Japan Institute of Electronics Packaging (JIEP). He has been also serving the Representative Director of Institute for Advanced Micro-system Integration (IMSI) in Japan.

DR. **YASUMITSU ORII**
NAGASE & CO., LTD. Tokyo, Japan

YASUMITSU ORII received the B.S. in Material Science from the Osaka University, Japan and the Ph.D. from the Osaka University, Japan as well. He had been worked in IBM for 30 years and he left IBM at the end of June/2016. He joined Nagase on July 1st and he is the general manager of New Value Creation office at Nagase. Before joining Nagase, he was the senior manager of IBM Research Tokyo Science & Technology division to lead the three projects which were 3D integration, Optical Interconnection and Brain Inspired Devices. He is “IEEE Senior Member” , “IEEE EPS Region 10 Director” and “IMAPS Fellow”.

DR. YASUSHI MASUDA

Fujitsu Advanced Technologies Limited

YASUSHI MASUDA is a manager of Packaging and Cooling Technology Dept. at FUJITSU Advanced Technologies Limited, Japan. He received Master degree in Mechanical Engineering from Nagaoka University of Technology, Niigata, Japan in 1999. His main field is the development for computer packaging technology at system level. He has been engaged in a lot of FUJITSU products with development and design verification from mechanical point of view. In particular he is specialized in interconnect components like electrical connectors, cables, optical modules. One of his recent interests is high speed Signal Integrity and Components to achieve next generation computer systems. The other is cooling technology, particularly immersion cooling, almost the same as important as Signal Integrity.

DR. HIDEYUKI NASU

Furukawa Electric Co., Ltd.

HIDEYUKI NASU received the B.E., M.E., and Ph.D. degrees from the College of Science and Technology, Nihon University, Tokyo, Japan, in 1993, 1995, and 2006, respectively.

In 1995, he joined Furukawa Electric Co. Ltd., Tokyo. He has worked for parallel-optical modules for optical interconnects. He is the Executive Engineer of the Laboratories for Fusion of Core Technologies, Chiba, Japan, as well as an Adjunct Lecturer of electrical engineering with the College of Science and Technology, Nihon University. He is an author or coauthor of 55 patents and more than 130 publications.

Dr. Nasu is a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE), a Senior Member of the Information and Communication Engineer (IEICE) of Japan, and the Mission Fellow of the Japan Institute of Electronics Packaging (JIEP). He has been serving a committee member of IEEE Electronics Packaging Society (EPS) Japan Chapter and the Program Chair of IEEE CPMT Symposium Japan (ICSJ). He has been also serving the Vice Chair of the Optical Packaging Technology committee of JIEP. He received the Technology Award in 2012 and the Best Conference Paper Award in 2016 from JIEP, and the Best Paper Award from ICSJ in 2016. He is a principal member of the Optical Internetworking Forum (OIF) and the Consortium for On-Board Optics (COBO).

DR. TOSHIHISA NONAKA

Packaging Solution Center, Hitachi Chemical Co., Ltd.

TOSHIHISA NONAKA graduated from the University of Tokyo in 1986 and received Ph. D degree in 1995 from Nagoya University. He has been working in the research of electronic materials more than 30 years. From 1986-2015 he had been worked in Toray industries. Since 2015 he has been a technical director of Packaging Solution Center of Hitachi Chemical. Current his research topic is process and material development of advance package regarding FO-WLP/PLP, 2.5D, 3D and so on.

Introduction To Fan-Out Wafer-Level Packaging

Tuesday, 4th December
<08:30am - 12:00pm>
Virgo 1

BY
DR. **BETH KESER**
Intel Corporation

Fan-out wafer level packaging (FO-WLP) technologies have been developed across the industry over the past 15 years and have been in high volume manufacturing for over 8 years. FO-WLP has matured enough that it has come to a crossroads where it has the potential to change the electronic packaging industry by eliminating wire bond and bump interconnections, substrates, leadframes, and the traditional flip chip or wire bond chip attach and underfill assembly technologies across multiple applications. This course will cover the advantages of FO-WLP, potential application spaces, package structures available in the industry, process flows, material challenges, design rule roadmap, reliability, and benchmarking.

Course Outline:

01 — Current Challenges in Packaging
02 — Definition and Advantages
03 — Applications
04 — Package Structures
05 — Process
06 — Material Challenges
07 — Equipment Challenges
08 — Design Rule Roadmap
09 — Reliability
10 — Benchmarking

Who Should Attend:

Engineers and managers responsible for advanced packaging development, package characterization, package quality, package reliability and package design should attend this course. Suppliers who are interested into supporting the materials and equipment supply chain should also attend. Both newcomers and experienced practitioners are welcome.

BETH KESER, Ph.D., a recognized global leader in the semiconductor packaging industry with over 20 years of experience, received her B.S. degree in Materials Science and Engineering from Cornell University and her Ph.D. from the University of Illinois at Urbana-Champaign. Beth's excellence in developing revolutionary electronic packages for semiconductor devices has resulted in 27 patents and patents pending and over 40 publications in the semiconductor industry. For over 7 years, Beth led the Fan-Out and Fan-In Wafer Level Packaging Technology Development and NPI Group at Qualcomm where she and her team qualified over 50 products resulting in over 8 billion units shipped--technology consumers around the world enjoy in cell phones today. Beth is also an IEEE EPS Distinguished Lecturer who chaired IEEE EPS's 2015 ECTC and is currently EPS's VP of Education. Based in Munich, Germany, Beth currently leads the Components and Systems Solutions Department at Intel Corporation in the Communication Device Group.

Advanced Integrated Circuit Design For Reliability

Tuesday, 4th December
<08:30am - 12:00pm>
Virgo 2

BY
DR. **RICHARD RAO**
Microsemi Corp, USA

This short course provides a holistic understanding of all aspects of reliability failure modes and mechanisms of an advanced IC product and the design for reliability methodology. It covers advanced Si process like FinFET, packaging technologies like Flip Chip BGA, Wafer Level packages, 2.5D/3D and interconnects like Cu pillar, TSV/uBumps and Cu/Cu hybrid bonding.

Course Outline:

01 — Introduction
Reliability models and statistics | Reliability challenges

02 — Advanced Si reliability issues
FinFET FEOL reliability | BEOL Cu/ELK reliability | BEOL and FEOL interactions

03 — Advanced packaging technologies and reliability failure mechanisms
Advanced packaging technologies including FCBGA, WLP &2.5D/3D, etc | TSV/uBumps, Interposer, Cu Pillar and Cu/Cu bond Related Failures | Interconnect migration failure under combined electrical current, thermal mechanical stress and temperature changes

04 — Chip to package interaction (CPI)
CPI basics | CPI simulations | CPI testing | Quantitative CPI reliability | Electrical CPI | Chip Board Package Interaction

05 — IC Design for Reliability
Reliability target and usage conditions | Reliability design rules | Design rule implementations

RICHARED RAO, Ph.D., is currently a Fellow of Microsemi Corp, a lead supplier of high reliability integrate circuit, located in southern California, USA and an elected Senior Member of IEEE. He is the present Chair of IEEE EPS (Electronics Packaging Society) Reliability Technical Committee. Dr. Rao is responsible for the corporate reliability and advanced packaging solutions. His focus is to find the advanced packages to meet the high performance, high reliability and high power semiconductor ICs; to study the new failure modes and mechanisms of cutting edge Silicon and packaging technologies as well as to develop design for reliability solutions for advanced circuits, packaging and chip to package interaction. He has a Ph.D. degree in solid mechanics of materials from the University of Science and Technology of China, the most prestigious university in China. Prior to joining Microsemi in 2004, Dr. Rao held various academic and technical positions in reliability physics and engineering. He was an associate professor at University of Science and Technology of China, a research fellow at Northwestern University, Evanston, IL, USA and a National Science and Technology Board Research Fellow in Singapore; and a principal engineer at Ericsson Inc. He has published over 30 papers on reliability physics and applications and a main contributor of several JEDEC standards. He is a technical committee member of IRPS (International Reliability and Physics Symposium) and ECTC (Electronics Component and Technology Conference). He is a frequent speaker to IRPS, ECTC, ISQED (International Symposium on Quality Electronics Design), ASME Symposiums and a keynote speaker to ICEPT and International Conf on System on Chip, etc. Dr. Rao has over 20 years' hands on experience and knowledge in silicon to package to system integration such as HKMG and FinFET, high performance FCBGA/CSP, WLP, 2.5D/3D, chip to package to board interaction, board and system level reliability physics and applications. He has conducted professional development courses on advanced IC reliability to both industrial and academic worlds.

3D Sip For Asic And Dram Integration

Tuesday, 4th December
<08:30am - 12:00pm>
Virgo 3

BY
DR. **LI LI**
Cisco Systems, Inc.

With the change in traditional IC scaling cadence, there is growing interest in system optimization and differentiation through 3-dimensional System-in-Package (3D SiP) technology for broad market applications including Artificial Intelligence (AI), High Performance Computing (HPC), Networking, and Internet of Things (IoT). Concurrently packaging technologies have still to meet the cost, performance, form factor and reliability goals. In this short course, we will examine the role of emerging 3D SiP packaging platform for addressing the gap seen between the slowdown of Moore's Law scaling and the ever-increasing system integration requirements. Systems based on 3D SiP technology have been developed for integrating high performance logic devices like Application-Specific Integrated Circuit (ASIC) and 3D High Bandwidth (HBM) Dynamic Random-Access Memory (DRAM) devices. We will review enabling packaging and interconnect technologies as well as new elements introduced by 3D SiP and potential risks to reliability of the final products. A detailed review on technology and component level qualification will be presented. It will then be followed by a few examples as case studies on board level reliability validation.

Course Outline:

01 — 3D SiP Introduction
02 — Enabling Technologies for 3D SiP
3D Stackable Memory | High Density Interposer i. Silicon Interposer, ii. Organic Interposer | Micro-bump Interconnect
03 — 3D SiP for ASIC and HBM DRAM Integration
Organic Interposer Design | Simulation and Results
04 — 3D SiP Assembly
05 — Test and Characterization
06 — Reliability Challenge
07 — Summary

Li Li, Ph.D., is a Distinguished Engineer at Cisco Systems, Inc. where he leads an initiative on 3D IC integration and advanced packaging development. He has been with Cisco since 2004 and has over 20 years industry experience in IC packaging design, technology development and qualification.

Dr. Li has published several book chapters and over 80 technical papers in the field of microelectronics packaging. He is on the Board of Governors of IEEE Electronics Packaging Society and the Board of Directors of HDP User Group International (HDPUG), Inc.

He received his M.S. and Ph.D. degrees in Mechanical Science and Engineering from the University of Illinois at Urbana-Champaign.

Understanding Flip Chip Technology And Its Applications

Tuesday, 4th December
<01:30pm - 05:00pm>
Virgo 1

BY
MR. ERIC PERFECTO
GLOBALFOUNDRIES

This course will cover the fundamentals of flip chip fabrication and assembly processes. It will include all aspects of SnAgCu solder bumping and Cu Pillar technologies, comparison of various under bump and joining metallurgies and their intermetallics, and solder deposition methods. It will cover interconnect technologies used in single and multi-die assembly in organic laminate packages, wafer-level packages, embedded die, chip-on-chip, chip-on-wafer and 2.5D/3D flip chip packages as well as examples of leading industry application. Advanced and current trend of flip chip assembly process are provided briefly. This course will cover the failure types and the analytical tools, such as sonoscan, solder or die shear, x-section, x-ray, EBSD, and shadow or projection moiré used for process monitoring and to identify defect root cause. Failure modes, such as barrier consumption, Kirkendall and other solder voids formation mechanisms, contact non-wets, BEOL dielectric cracking, electromigration, etc. will be included dispersedly in course.

Course Outline:

01 — Introduction to Flip Chip Technologies
02 — UBM Metal Selection and Solder Deposition Processes
03 — C4 and Cu Pillar Fabrication Issues
04 — Flip Chip Ball Grid Array (FCBGA) Assembly Process Flow
05 — Chip Package Interaction and Electromigration
06 — Flip chip technology new trends: Wafer Level, and 2.5D/3D
07 — Substrate Technologies and Characterization Methods

Who Should Attend:

The targeted audience includes scientists, engineers and managers currently using flip chip technology (w/solder or Cu Pillar) or considering moving from wire bonding to flip chip, as well as reliability, product or applications engineers who need a deeper understanding of flip chip technologies: the advantages, limitations and failure mechanisms.

ERIC PERFECTO has 36 years of experience working in the development and implementation of advanced packages. He is currently Principal Member of the Technical Staff at GLOBALFOUNDRIES. He holds an M.S. in Chemical Engineering from the University of Illinois and an M.S. in Operations Research from Union College. Eric has published over 75 papers, holds over 45 US patents, He has been honored with two IBM Outstanding Technical Achievement Awards, one for the Development and Implementation of Multi-Level Thin Film Structures, and the second for Development and Implementation of 150 um pitch C4. He also received an IBM Outstanding Contribution Award for the Development of 3D Wafer Finishing Process. Eric was the 57th ECTC General Chair in Reno, NV, and the Program Chair at the 55th ECTC. He is an IEEE Fellow, a Distinguish Lecturer of the EPS society of IEEE, EPS BoG member and the current EPS Awards Program Director.

Eric's recent areas of focus is the development and implementation of electroplated C4 and Cu pillars at GLOBALFOUNDRIES, and the assembly of Si photonics packages. His interest is in metallurgy effects on package reliability, design for manufacturability and yield improvements

Introduction To 3D Interconnect And Packaging Technologies

Tuesday, 4th December
<01:30pm - 05:00pm>
Virgo 2

BY

PROF. SARAH KIM
Seoul National University of
Science and Technology

3D interconnect and packaging technologies have been developed across the industries and universities over the past 20 years. 3D products with TSV (through Si via) have been in high volume manufacturing for over 5 years, which has the great potential to change the heterogeneous or high IO device packaging applications by improving power delivery, bandwidth, and latency and reducing a package size. This course will provide the introductory overview of 3D interconnect and packaging technologies. The technical trends and drivers, motivations, fabrication processes, stacking methods, benefits, and technical challenges will be discussed.

Course Outline:

01 — Technical trends and drivers
02 — Motivations
03 — Core fabrication processes
TSV (through Si via) | SI thinning | Bonding (including Cu-to-Cu wafer bonding)
04 — Stacking methods
05 — Technical challenges
Power delivery | Thermal management | Reliability | Yield (wafer level stacking)

Who Should Attend:

This course is intended for engineers who are new to this field, technical managers and scientific researchers who are interested in developing new technologies and products, and graduate students who are involved in advanced packaging process, design, and materials,

SARAH E. KIM, Ph.D., a professor at the Seoul National University of Science and Technology (Seoul Tech), received her B.S. in Materials Science and Engineering from Rensselaer Polytechnic Institute and her M.S. from Massachusetts Institute of Technology and her Ph.D. from Rensselaer Polytechnic Institute. Prior to join Seoul Tech, Sarah worked at Samsung Electronics, Intel, and Korea Institute of Science and Technology. In Intel she has worked on various areas of BEOL interconnect, 3D integration, and die-package interface development including liquid cooling, thick metal interconnect, and decoupling capacitor. Also, she led multiple wafer level package projects and managed a sort test group. At Seoul Tech, Sarah has been focusing her research on the development of 3D wafer packaging, fan-out wafer level packaging, and transparent oxide semiconductor. She holds more than 30 US patents including one of Intel's 45nm-node core patents and has numerous technical papers in international journals and received many honors and awards over the years (http://www.esl-seoultech.kr).

Power Electronic Packaging Reliability, Materials, Assembly and Simulation

Tuesday, 4th December
<01:30pm - 05:00pm>
Virgo 3

BY

DR. **NING-CHENG LEE**
Indium Corporation

DR. **YONG LIU**
ON Semiconductor Corp

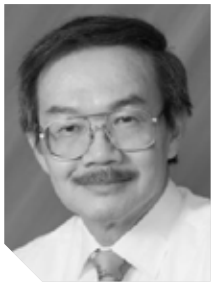
PROF. **SHENG LIU**
Wuhan University

For power electronic devices, the die attach is primarily conducted with the use of high lead solder alloys. The reliability of the joints depends on the detailed design, particularly the UBM structure on the die side. On the other hand, the move toward lead-free has driven the introduction of Sn-based Pb-free solder alloys and Ag or Cu sintering materials. While the lead-free solder alloys may have a lower service temperature but a higher electromigration resistance, the sintering materials offer outstanding thermal and electrical conductivity, a and very high service temperature. In this course, those bonding materials will be introduced and discussed in detail.

Due to the intrinsic structural nature, the requirement for power product and its reliability is extremely high. This talk will present the overview of advances in power electronic packaging. A review of recent advances in reliability of power electronic packaging and modeling is presented based on the development of power electronics. The talk will cover in more detail of advanced modeling for reliability issues in both assembly manufacturing process induced reliability and the reliability tests. Along with power packaging development, the role of simulation in codesign and virtual prototype is a key to assure successful new power electronic packaging.

Modeling and simulation of microelectronic packaging and assembly is a multi-disciplinary activity that relies on the expertise of sequence dependent complex processes, almost all the material types, and detailed process windows; a very challenging task for both academic people and practicing engineers. The most popular methodology of design and manufacturing is called Design for X (DFX, here X refers to manufacturing, assembly, testing, reliability, maintenance, environment, and even cost). A packaging module and related application systems, like any other electronic systems, involve a lot of manufacturing processes from crystal growth, film deposition, etching, chip to wafer and wafer to wafer bonding, dicing/ sigulation, and extensive reliability testing for extended-life goals. Design procedure must be modified and DFX must be used so as to achieve prevention with integrated consideration of manufacturing processes, testing, and operation. The talk will focus on the many detailed processes in front end, back end, even probing, wire bonding, bonding, and so on. It covers the broad aspects from manufacturing to reliability, and to testing, with many examples. This talk can provide guidance to those in the field and present a design approach that must ultimately replace the build-test-fix-later process if the efficiencies and potential cost benefits of the microelectronic packaging systems are to be fully realized.

Ning-Cheng Lee, Ph.D. is the Vice President of Technology of Indium Corporation. He has been with Indium since 1986. Prior to joining Indium, he was with Morton Chemical and SCM. He has more than 30 years of experience in the development of fluxes and solder pastes for SMT industries. In addition, he also has very extensive experience in the development of underfills and adhesives. He received his PhD in polymer science from University of Akron in 1981, and BS in chemistry from Taiwan University in 1973.



Ning-Cheng is the author of "Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP, and Flip Chip Technologies" by Newnes, and co-author of "Electronics Manufacturing with Lead-Free, Halogen-Free, and Conductive-Adhesive Materials" by McGraw-Hill. He is also the author of book chapters for several lead-free soldering books. He received 1991 award from SMT Magazine and 1993 and 2001 awards for best proceedings papers of SMI or SMTA International Conferences, 2008 and 2014 awards from IPC for Honorable Mention Paper – USA Award of APEX conference, and 2010 Best Paper Award of SMTA China South Conference. He was honored as 2002 Member of Distinction from SMTA, 2003 Lead Free Co-Operation Award from Soldertec, 2006 Exceptional Technical Achievement Award from CPMT, 2007 Distinguished Lecturer from CPMT, 2009 Distinguished Author from SMTA, 2010 Electronics Manufacturing Technology Award from CPMT, 2015 IEEE Senior Member, 2015 Founder's Award from SMTA, and 2017 IEEE Fellow. He has served on the board of governors for CPMT and SMTA board of directors. Among other editorial responsibilities, he serves as editorial advisory board of Soldering and Surface Mount Technology, Global SMT & Packaging and as associate editor for IEEE Transactions on Components Packaging Manufacturing Technology. He has numerous publications and frequently gives presentations, invited to seminars, keynote speeches and short courses worldwide on those subjects at international conferences and symposiums.

Dr. Yong Liu has been with ON Semiconductor Corp in South Portland, Maine since Sept, 2016 as a Principal Member of Tech Staff. Before Fairchild was acquired by ON Semiconductor, he worked at Fairchild Semiconductor as a Distinguished Member Technical Staff. His main interest areas are advanced analog and power electronic packaging, modeling and simulation, reliability and material characterization. He was elevated as IEEE fellow in 2015.

Prof. Sheng Liu Sheng Liu, Ph.D. is the dean of the School of Power and Mechanical Engineering and the Institute of Technological Science of Wuhan University. He is the National Science Fund for Distinguished Young Scholars (Type B), Yangtze River Scholar Distinguished Professor, ASME Fellow, IEEE Fellow, and as a professionalism in the area of the "863 program" of the National High Technology Research and Development Program. He has acquired his doctor degree in Stanford University in 1992. From 1992 to 1995, he held the title of lecturer at Florida institute of technology. He was authorized as a tenure from 1995 to 2001 in the Department of Mechanical Engineering and manufacturing research at Wayne State university. During the period of his title job, his outstanding achievements in the research of the reliability of complex structure of IC packaging, he was granted the President's prize of the United States of America. The research of IC and MEMS packaging with the research of CAD allowed him to obtain the Young Investigator Award in Natural Sciences of the United states of America. In 2001, Sheng Liu resigned from the Department of Mechanical Engineering and Manufacturing research at Wayne State University and returned to China, where he took the lead of carrying out research focusing on the theory of Reliable Engineering Development for electronic packaging.

Invited Presentation

Packaging for Performance Scaling

Thursday, 6th December
<08:30am - 09:00am>
Gemini 2

BY

MR. **SAM KARIKALAN**
Senior Manager,
Broadcom

Slowing down of Moore's law has forced the industry to come up with innovative ways of scaling up semiconductor device performance with the help of heterogeneous integration packaging technologies. Process technologies for Substrates, Silicon Interposers, Through-Silicon-Vias and Fan-Out packaging that are needed for such high end packaging, are all slowly maturing towards high yields. However the Electrical, Thermal and Mechanical performance demand for these package types will keep growing steadily in the coming years, as the end use applications of these devices constantly push the envelope on speed and power. This talk would present the design challenges posed by such performance needs and discuss the areas that need to be jointly addressed by the design, materials and process engineering communities to be fully prepared.

SAM KARIKALAN is a Senior Manager at Broadcom Inc., Irvine, California, leading a global team of Signal Integrity, Thermal and Mechanical design experts that is responsible for package design optimization for performance in networking, broadband, storage, wireless and mobile devices. Sam has been with Broadcom for over 13 years. Prior to that, he worked for STATS ChipPAC, Primarion and Advanced Micro Devices on electrical modeling and characterization, package design optimization for electrical performance and component level EMI. The first ten years of Sam's 31 yearlong industry experience was on System Level EMI/EMC at SAMEER-Centre for Electromagnetics in India, being responsible for EMC Compliance Testing, EMI fixes and EMC Design. Besides package design optimization for SI/Thermal/Mechanical performance, Sam is also currently working on Package Technology Development for Performance Scaling, such as 2.5D Integration, extensively working with the supply chain. He has 22 issued US patents and several papers in International Conferences/Journals to his credit. He is a Senior Member of the IEEE and a Member-at-Large on the Board of Governors of the IEEE Electronics Packaging Society. Sam also served as the General Chair of the 2018 IEEE Electronics Components and Technology Conference (ECTC), held in San Diego, California this year.

Three-Dimensional Embedded Capacitor in Through-Silicon Via (TSV)

Thursday, 6th December
<08:30am - 09:00am>
Leo 1

BY

PROF. **CHUAN SENG TAN**
School of Electrical and Electronic Engineering
Nanyang Technological University

A novel integrated capacitor, called "three-dimensional (3-D) embedded capacitor" is proposed, designed, fabricated, and characterized for application in integrated circuits (ICs) with through-silicon vias (TSVs). A significant capacitance density enhancement can be achieved for this 3-D embedded capacitor, because it leverages on the existing TSVs. Compared to conventional trench capacitor, this technology does not consume additional silicon area because it is embedded in the trenches of TSVs, instead of in the dedicated trenches. Firstly, two types of 3-D embedded capacitors are designed with different electrode deposition methods. The atomic layer deposition (ALD) type 3-D embedded capacitor features an extremely high capacitance density for high-end applications, whereas the sputtering type 3-D embedded capacitor features a higher electrode deposition rate and ease of integration for low-cost applications. Secondly, an electrical model of the 3-D embedded capacitor is constructed with analytical equations to predict its capacitance based on the physical design parameters. An ultra-high capacitance density, 5,621.8 nF/mm2, can be envisioned for the 3-D embedded capacitor in the trench of a TSV with a diameter of 50 μm and a depth of 30 μm. In addition, a finite element simulation is performed to ensure the structural integrity of the 3-D embedded capacitor and its surrounding components. The simulation result shows that the maximum thermo-mechanical stress changes only slightly from 1567.8 to 1576.8 MPa when a 3-D embedded capacitor is included. Next, prototypes of 3-D embedded capacitors are fabricated successfully with an optimized process flow design and implementation. After the fabrication, cross-sectional scanning electron microscope (SEM), transmission electron microscopy (TEM), and energy-dispersive X-ray spectroscopy (EDX) are performed on both ALD type and sputtering type test vehicles. The SEM and TEM pictures show ~100% step coverage of ~50 nm TiN and ~10 nm Al2O3 layers for ALD type test vehicles but poor step coverage of TiN layer for sputtering type test vehicles (the thickness drops from 400 nm on the top surface to 200 nm on the top part of the sidewall). The EDX line-scans across the stacked layers provide semi-quantitative proof of correct stoichiometry of the TiN/Al2O3/TiN/SiO2/Si layers. Lastly, capacitance-voltage (C-V) and current-voltage (I-V) characterizations are performed to evaluate the electrical performance of the test vehicles of 3-D embedded capacitors. The C-V characterization results show that, as the trench diameter increases from 10 to 50 μm, the capacitance density of 3-D embedded capacitors increases from 98.7 to 625.2 nF/mm2 for ALD type test vehicles. It also increases from 3.6 to 138.7 nF/mm2 for the sputtering type test vehicles. These measurement results of the ALD type test vehicles are found to be in good agreement with the corresponding electrical modelling results, which are calculated based on the analytical equations derived early in the study. However, this is not the case for the sputtering test vehicles. The difference is probably due to the super conformal step coverage of electrodes provided by ALD and the poor step coverage of electrodes provided by sputtering. From the I-V characterization results, it can be observed that the leakage currents of the ALD type embedded test vehicles do not deviate from those of their planar capacitor counterparts, but the leakage currents of the sputtering type embedded test vehicles degrade from the leakage currents of their planar capacitor counterparts. The suspected cause is the rough trench sidewall due to sputtering deposition method. The current density (J-E) results show that the leakage current density is ~2×10-7 A/cm2 at 2 MV/cm and the dielectric strength is ~9.7 MV/cm for the ALD type test vehicles; whereas the leakage current density is ~3×10-9 A/cm2 at 2 MV/cm and the dielectric strength is ~8.0 MV/cm for the sputtering type test vehicles. This technology is promising in integration of ultrahigh-density on-chip capacitor. The above merits will pave the way for on-chip energy storage element, integrated voltage regulator, capacitively coupled wireless module and many other possibilities. Authors are grateful for funding support from A*STAR Quantum Technology for Engineering (A1783c0004).

CHUAN SENG TAN received his BEng degree in electrical engineering from University of Malaya, Malaysia, in 1999. Subsequently, he completed his MEng degree in advanced materials from the National University of Singapore under the Singapore-MIT Alliance (SMA) program in 2001. He then joined the Institute of Microelectronics, Singapore, as a research engineer where he worked on process integration of strained-Si/relaxed-SiGe heterostructure devices. In the fall of 2001, he began his doctoral work at the Massachusetts Institute of Technology, Cambridge, USA, and was awarded a Ph.D. degree in electrical engineering in 2006. He was the recipient of the Applied Materials Graduate Fellowship for 2003-2005. In 2003, he spent his summer interning at Intel Corporation, Oregon. He joined the School of Electrical and Electronic Engineering, Nanyang Technological University, in 2006 as a Lee Kuan Yew Postdoctoral Fellow and since July 2008, he was a holder of the inaugural Nanyang Assistant Professorship. In February 2014, he was promoted to the rank of Associate Professor (with tenure). His research interests are semiconductor process technology and device physics. Currently he is working on process technology of three-dimensional integrated circuits (3D ICs), as well as engineered substrate (Si/Ge/Sn) for silicon photonics. He has numerous publications (journal and conference) and IP on 3D technology and engineered substrates. He has co-edited/co-authored four books on 3D packaging technology. He provides his service as committee member for International Conference on Wafer Bonding, IEEE-3DIC, IEEE-EPTC, IEEE-ECTC, IEEE-EDTM, and ECS-Wafer Bonding. He is an associate editor for Elsevier Microelectronics Journal (MEJ) and IEEE Transactions on Components, Packaging and Manufacturing Technology. He is a member of IEEE.

Soldering Material Challenges For Heterogeneous Integration And Assembly

Thursday, 6th December
<08:30am - 09:00am>
Leo 2

BY

MS. **LIM SZE PEI**
Regional Product Manager - Semiconductor
Indium Corporation

With the industry's continuous push towards miniaturization, increased functionality, lower power consumption, lower cost, and faster time-to-market, heterogeneous integration is seen as one of the best solutions moving forward. As defined by ITRS, heterogeneous integration refers to the integration of separately manufactured components into a higher-level assembly, such as System-in-Package (SiP), which provides enhanced functionality and improved operating characteristics in the aggregate. As this integration becomes more extensive and the assembly process becomes more complicated, different types of soldering alloys and fluxes are often needed to meet the processing and reliability requirements. There may be step reflow soldering involved for some SIP assembly processes to attach different components at different processing steps, where the substrate needs to go through multiple reflow cycles. In order to reduce solder joint remelt issues, different alloys with different melting points are being explored, typically ranging from a low-melting alloy with a melting point around 130-160oC, to a middle melting range alloy of 170-200oC, and finally to the typical SAC305 or Sn rich alloy which melts around 215-260oC. Other than melting points of the alloy, the basic properties of the alloy must be taken into consideration for different applications as well. Due to the drive towards miniaturization, such as the deployment of passive component size down to 008004 (0.25 x 0.125mm) and smaller, or wafer level CSP (WLCSP) with small pad designs of less than 100um in diameter, solder paste with finer powder sizes of type 6 (5-15µm) or even type 7 (2-11µm) are required to create good solder joints. Though it is more challenging to handle solder paste with finer powder size compared to the conventional type 3 (25-45µm) and type 4 (20-38µm), due to higher oxidation potential, a fine powder solder paste with the key attributes of good wetting performance, low-voiding, good graping resistance, and good slump resistance to minimize bridging down to 50um gap, is still expected to have a long and stable working life. On the other hand, higher density design combined with reduced bondline thickness or standoff of flip-chip or other IC packages, makes cleaning flux residue more challenging. If the flux residue is not properly cleaned, it may cause delamination issues if it is not compatible with the molding or underfill material which will be used in the subsequent process. Some of the flux residue that is left behind, especially the water-soluble type, can even cause corrosion issues. Therefore, the shift towards using semiconductor-grade ultra-low residue no-clean fluxes, which eliminates the cleaning process, is the solution for overcoming these challenges. The flux residue left behind after the soldering process is minimal and compatible with the underfill or molding material. Thinner package, thinner die with high I/O count, comes with the warpage challenge. Different types of bonding technologies, such as Thermo-Compression Bonding (TCB) or Laser-Assisted Bonding (LAB), are being investigated to increase the production yield. Such bonding technologies typically heat-up the solder in a very short time (often seconds) to create the solder joint. This is another consideration that must be taken in order to choose the correct flux that has minimal spattering and good wetting with short activation time. All these challenges will be discussed in the presentation.

SZE PEI LIM is the Regional Product Manager for Semiconductor Products and is based in Malaysia. She manages the semiconductor product lines for the Asia region and works closely with the internal sales and R&D teams to develop solutions for industry needs and requirements. She also collaborates with external customers and corporate partners to support the industry's move towards heterogeneous integration. Some of her recent work includes the development of materials and processes for advanced packaging for fine feature printing targeted at the SiP application, as well as for one-step OSP ball-attach application. Sze Pei has more than 25 years of experience, specifically in the areas of PCB assembly and surface mount technology. She joined Indium Corporation in 2007 as a Technical Manager in Southeast Asia. Prior to that, she was a research and development chemist, focusing on solder paste and flux formulation. Sze Pei also worked as a technical manager at Inventec for nine years, where she provided technical support and managed testing in the lab. Sze Pei earned her bachelor's degree from the National University of Singapore, where she majored in industrial chemistry with a focus in polymers. She is an SMTA-certified Process Engineer, has earned her Six Sigma Green Belt designation, and is heavily involved in many research and roadmapping organizations.

Emerging NAND Memory Packaging Challenges

Thursday, 6th December
<08:30am - 09:00am>
Leo 3

BY

DR. **GOKUL KUMAR**
Principal Engineer in Packaging & Assembly Group, Western Digital

NAND Flash is the primary storage of choice for smart phones, tablets and solid-state drives. The electrical requirements for this memory has exponentially evolved from its original multimedia consumer applications (with uSD cards, USB, audio players, cameras, cell phones) into enterprise storage and server farms. In this latter space, it has become an indispensable component in the memory hierarchy of large storage systems. Penetration into these markets is fueled through a relentless improvement in cost per bit by two factors: a) Migration to 3-D monolithic NAND fabrication process and b) Aggressively growing the number of dies stacked using advanced packaging techniques, from 1 die in 2003 to 16 dice in 2014..A roadmap based on 3-D monolithic NAND process has created situation where the ability to predict technology behavior is no longer solely based on scaling lithography. Rather, each node is connected to a combination of parameters such as cell diameter, vertical cell pitch, numbers of cells in a stack and the number of bits per cell. While both these factors independently cause well-established packaging challenges, their intertwined interactions have resulted in addition considerations. Stacking more memory dice within a given package height or to reduce package thickness continues to reduce individual die thickness. Such thinner die has lower rigidity, larger warpage, and poorer strength. The arising challenges from thin die assembly and device reliability of extremely thin NAND memory dies have been discussed based on our experimental and simulation studies. Modeling methods to predict arising warpage arising from corresponding substrate thinning has also been published. This paper presents an overview of critical challenges from a) materials, b) process, and c) design of NAND packages and proposes solutions based on experimental and analytical studies. In this work, the first section examines critical processing challenges due to thin die stacking. The process of mechanical saw spin dicing on the very thin flash creates chip out (particles), micro-cracks start to propagate and impact active circuit zone. This paper explores tighter thickness tolerances on back-grinding equipment, including optical dicing methods. The use of high modules DAF materials to prevent cracking from thin-die at overhang locations as a part of the die stack is also studied. A combination of more than 4 different categories of materials is used in semiconductor packages, including semiconductor material, metals, organic polymer and dielectric materials. The subsequent section analyzes the warpage challenges specific to NAND stacking die and substrate materials. The EMC compound selection and improvement opportunities to enable overall thin packages is analyzed. The final section examines design challenge arising from the technical point of view on substrate design and integration of ASIC flip-chip dies along with NAND memories. In addition, additional unknowns in NAND 3-D integration using TSVs present from both cost and technology perspective are discussed.

GOKUL KUMAR is a Principal Engineer with the Packaging & Assembly Group at Western Digital, Milpitas, USA. He has a multi-disciplinary expertise in the areas of packaging of electronic systems, signal and power integrity, 3-D integration. Previously, he worked on developing 3-D interposers within the glass/silicon interposer consortia at the 3-D packaging research center in Georgia Tech. He has coauthored about 15 conference and journal publications, with 1 issue patent and 5 others pending. He regularly reviews papers for IEEE CPMT, and several other conferences including EPEPS, International Midwest Symposium on Circuits and Systems, etc.

He received his PhD and MS specializing in Electrical and Computer Engineering, from the Georgia Institute of Technology in 2015 and 2010 respectively.

Microfluidic Electroless Interconnection Process for Low-Temperature, Pressureless Chip-stacking

Thursday, 6th December
<08:30am - 09:00am>
Leo 4

BY

PROF. C. ROBERT KAO
Program Manager, Ministry of
Science and Technology of Taiwan

Increasing demands for high-performance miniaturized electronic devices have driven the semiconductor industry toward finer pitch and higher interconnect density. Copper pillar has been widely adopted and is rapid becoming the mainstream bumping technology for high-density interconnections, such as 2.5D and 3D IC packaging. Thermo-compression bonding has been widely used for high-density copper pillar bumps because of its highly accuracy alignment and placement. However, the high heat and high force applied to the components during the bonding process often induce high thermal-mechanical stress that causes severe damage to the devices and low-k dielectric layers. Because the mechanical properties of porous, low-k materials decreases with lower dielectric constants, this issue will become more severe in the future when lower dielectric constant materials are employed. Therefore, it is imperative to develop a low-temperature, low-pressure bonding process.
To address this issue, a novel Cu-to-Cu bonding process called microfluidic electroless interconnection has been developed. This novel process forms electroless metal interconnections as a replacement for solders, which eliminates all the reliability concerns involved with soldering. Specifically, the process is able to bond copper pillars at a low temperature without applied any pressure. The operating temperature of the process is around 80 °C, which is considerably lower than most bonding processes. Also, there is no need to apply any bonding pressure throughout the bonding process due to the proposed bonding scheme structure. In this way, the thermo-mechanical stress can be largely reduced to maintain the structural stability of packaging. Furthermore, the most exciting aspect of this new approach is the integration of microfluidic technology with the electroless plating process, which allows to precise control the flow of fluids in and out the stacked chip to achieve better bonding performance. The flow rate can quantitatively determined and the fluid flow can be adjusted for either batch or continuous-flow operations. The main objective of this work was to investigate the feasibility of the microfluidic electroless interconnection process in joining copper pillars as a promising route for a low-temperature, pressureless bonding process. First, the overall plating uniformity across the entire die surface at different stand-off heights of the stacked chips was investigated. Preliminary results demonstrated that, by selecting a proper flow rate, a high level of plating uniformity across the die was obtained regardless of the standoff heights. In addition to the electrolessly bonded joints, when the bonding interface was examined by scanning electron microscopy (SEM) and focus ion beam (FIB), it was confirmed that no voids or seams appeared on the bonding interface between the pillars, indicating that the two electroless Ni layers that grew on the opposite sides had merged completely into a single structure. The growth and bonding mechanism of the electroless interconnection process was investigated and characterized fully. The bonding interface and phosphorus distribution in the electroless Ni bonds were examined by an electron probe micro-analyzer (EPMA) to ascertain the effect of batch and continuous flow processing. Moreover, the results of direct shear test shows that the bond strength of the electroless Ni between the copper pillars was greater than the adhesion strength of the Cr layer. Further, it was found that the process has the ability to compensate not only for non-uniform copper surfaces, but also for the misalignment and height mismatch of copper pillars, which provides a competitive edge over other bonding methods. This innovative low-temperature, pressureless electroless bonding approach shows considerable promise for applications that require low stress and low thermal budget process.

C. ROBERT KAO received his PhD in Materials Science from University of Wisconsin-Madison in 1994. He joined National Central University (Taiwan) in 1995 as an assistant professor. In 2005, he became the first director for the newly established Graduate Institute of Materials Science & Engineering at National Central University. In 2006 he relocated to National Taiwan University, became a University Distinguished Professor in 2008, and served as the Department Head of Materials Science and Engineering from 2010 to 2013. He currently also serves as the program manager of Materials Engineering in Ministry of Science and Technology of Taiwan. His main research interests include electronic, optical, and MEMS packaging with a main thrust on the thermodynamics and kinetics of materials interactions within packages. He helped organizing 16 international symposia on solders and soldering technology for TMS and ASM. He has served as guest editors for Journal of Electronic Materials and Microelectronic Reliability, and currently is a Principal Editor for Journal of Materials Research and Associate Editor for Journal of Materials Science – Materials in Electronics. Kao is a committee member for CPMT Materials and Processing Technical Committee, and also served as session chair for ECTC meeting. Kao is a Fellow of the ASM and MRS-Taiwan. In 2014, he received the Brimacombe Medalist Award from TMS. He is a High Impact Research Icon of University of Malaya, Kuala Lumpur. He has authored over 130 referred journal papers, five of which reached the status of Highly Cited Papers according to Web of Science Essential Science Indicators. He has an h-index of 33. He holds 10 US and Taiwan patents. Kao is considered the leading experts on the metallurgical reactions for electronic packaging applications, and has given more than 30 invited or keynote lectures in international conferences. He presented an invited talk at the Gordon Research Conference (Plymouth State College, July 23-28, 2000), and served as a discussion leader for the same conference in 2006. In addition to his teaching and research activities, Professor Kao was an independent board member of LOTES (2006-2010), and served as consultants for many industry leading corporations, including ASUS and VIA Technologies.

Submicron Polymer Re-distribution Layer Technology for Advanced InFO Packaging

Thursday, 6th December
<01:50pm - 02:20pm>
Gemini 2

BY

DR. **HAN-PING PU**
Deputy Director of Advanced Packaging, TSMC

High-performance computing (HPC) applications such as Artificial Intelligence (A.I.) have been the hot topic in recent years. The advanced multi-chip packaging plays an important role for fast time-to-market and cost effective solution instead of SOC. For the increasing bandwidth requirement, more I/O die to die communications for advanced packaging is a need. To fulfill this demand, large number in registered routing lines between dies lead a constant drive for miniaturization for die to die Redistributed Layer (RDL) among industry. To achieve this, it is undoubtedly to induce the demand of dimensional scalability on line-width and corresponding via size of die-to-die interconnects, to be deployed for providing more communications between chips. In this talk, InFO Ultra-High-Density (UHD) RDL technology is presented for die-to-die communication with RDL line-width down to submicron range (<1um) [1, 2]. It is preferable to be designed to manufacture from packaging-industry available tool sets instead of Cu/low-k in BEOL counterpart, to ensure competitiveness in cost to other techniques in current commercial market. Accordingly, for this technology, Cu RDL and Cu via are deployed by PVD barrier/seed with following electro-plating process, plus sufficient process support from etching, ash, and lithography to realize the designed fine line dimensional architecture consisted of two RDL layers at least. All tool sets have been intentionally and initially arranged from current commercialized industrial packaging available processing and metrological tools with necessary retrofit, for both purposes of cost consideration and process adopted availability. The InFO UHD RDL technology is characterized by electrical performances, e.g., via-chain continuity, RDL Comb/Meander Rs, line-to-line leakage current, and eventually interconnect reliability testing such as electro-migration (EM), stress migration (SM), breakdown voltage (Vbd), Time-Dependent-Dielectric Breakdown (TDDB), etc. After process optimization, the electrical test data demonstrate >99% yields from via-chain continuity, RDL Comb/Meander Rs and leakage current. Initial interconnect reliability testing shows good performance from EM, SM, Vbd, TDDB, etc. Our UHD line and via EM performances are compatible to commercial L/S 2/2um, 5/5um, and 10/10um RDL EM performances. SM results pass TSMC internal criteria for UHD technology under via SM of Via 1.5um, and also for the case of both line/via SM in the L/S 1/1um with Via 2um. For Vbd and TDDB, we conduct the wafer-level testing under relatively severe conditions, as Vbd at 125oC with ramping stressed voltage rate of 1V/0.5 sec from 0 to 100 volts, and TDDB at constant 200 volts at 125oC. Even under these conditions, both Vbd and TDDB data still pass without failure. For InFO level reliability test, the torturing condition is employed as MR (Multiple Reflow) before deploying electrical properties measurement. It is evident that all MR samples pass the criteria without any failure. Furthermore, we conducted TCB 700 cycles (-55oC to 125oC thermal cycling condition) and recognize no failure occurred as well. Heading to miniaturization furthermore of RDL dimension in the future for various applications and benefits of more inter-chip communication paths, possible materials change, for instances of RDL dielectric materials, molding materials, and lithographic photoresist materials, etc., would definitely be included in any look-ahead plan. Low-temperature process based dielectric materials would be popular to fulfill flexibility in various applications of inter-chip connections, such as logic to memory die combination in one package. Meanwhile, for any new approaches including both materials change and innovative integration flow proposals, simulation always provides a handy methodology for us to determine strategically any possibility beforehand. Additionally, both process and metrological tools of current phase might need to be retrofitted or even be re-developed. Furthermore, any approach to enhance line or via strength, or to boost EM/SM performances are definitely welcome. Many similar examples can be seen or predicted, and we might even face some unknown challenges as miniaturization technology evolution continues in the future.

HAN-PING PU received Ph.D. degree in Materials Science and Engineering from National Sun Yat-Sen University, Kaohsiung, Taiwan, in 1995. He devoted himself to the field of semiconductor packaging for over 20 years. His career is mainly focus on advanced packaging development, package modeling and resolving chip-package interaction issues. He is now a Deputy Director of Advanced Packaging Division in TSMC R&D, Hsinchu, Taiwan. He has been involved in the invention of over 80 US patents and published more than 10 technical papers in semiconductor packaging area. He is an IEEE and EPS member.

A Framework for Reliability Assessment of Chemical-Induced Display Delamination

Thursday, 6th December
<01:50pm - 02:20pm>
Leo 1

BY DR. KEDAR HARDIKAR
Module Reliability
Engineering Lead, Google

Touch-enabled displays in handheld and wearable devices are expected to meet aggressive design requirements in harsh use conditions. The use conditions include exposure to household chemicals like sweat, hand lotion, sunscreen in addition to high temperature and high humidity conditions. Typical applications include smart phones, smart watches, touch bar of a MacBook Pro, and tablet PCs. This study examines chemical induced interfacial delamination within a display module. A typical display stack up consists of cover glass, optically clear adhesive, polarizer, touch panel, pressure sensitive adhesive, poly-imide based pOLED, PET film, and conductive adhesives. The lamination process, which varies from one display manufacturer to the other, typically leaves the display stack in a state of internal stress. Other than the cover glass, the edges of the display stack are susceptible to degradation due to exposure to chemicals. Conventional approach to address the degradation risk is to develop product design constraints (example: enclosure) that provide sufficient resistance to ingress of chemicals and moisture. However, Industrial Design requirements of lighter weight and slimmer form factors may prevent successful protection of the edge of the display stack. Hence, characterization of chemical induced delamination failures is critical for display reliability assessment. In this work experiments are conducted with the display edge exposed to specific chemicals. This is considered to be a limiting case of chemical exposure for display module edge. It is observed that in this test the delamination is typically initiated at a point along the edge and proceeds as an approximate semi-elliptical crack front. It is further observed that the growth rate of the crack front diminishes exponentially with time, and the crack attains a limiting dimension. Furthermore, accelerated testing carried out at elevated temperature and humidity conditions shows that the crack growth has the same exponential behavior. The observed delamination can be modeled as a semi-elliptical interfacial crack front. If such delamination is driven primarily by internal stresses the energy release rate for the delamination decreases as the delamination size increases and hence such delamination would be self-limiting where the limiting size is a function of the magnitude of internal stresses and the conditions to which the display stack is subjected in the test. This is consistent with the observed delamination failures. The observed delamination induced in this test can be modeled as a semi-elliptical interfacial crack front. Based on classical fracture mechanics, crack growth occurs when strain energy released during crack growth exceeds the energy required for the creation of the new fracture surface. The semi-elliptical crack front suggests that the crack growth is driven by stresses that are almost isotropic. High magnification photos of the crack front show the dendritic features typical of internal stress driven delamination. Hence, internal stresses within the display stack up, induced by the lamination process, is considered to be the primary driver of this interfacial crack. Creation of a new fracture surface (crack growth) relieves the internal stresses in the display stack, thus decreasing the incremental energy available for creation of new surfaces. This reduces the crack growth rate in an asymptotic manner till it reaches it limiting dimension. While fracture energy considerations can be used to understand the self-limiting nature of such delamination, temporal evolution of such defects is not easily amenable to analysis. Since a theoretical analysis is beyond the scope of this paper, an empirical equation is proposed to describe the evolution of interfacial delamination with time. The proposed relation is shown to describe the experimental data satisfactorily. Such quantification of the time-evolution of delamination enables evaluation of different display stacks in a structured manner. Finally, it is shown that this characterization framework can enable an enhanced reliability assessment of the module reliability data.

KEDAR HARDIKAR is the Module Reliability Engineering Lead (Mechanical) for products developed by Google's Consumer Hardware division. In addition, he is an adjunct faculty member at San Jose State University,California. He holds a Ph.D in Solid Mechanics from the Division of Engineering, Brown University, and has over 10 years of technical leadership experience in semiconductor capital equipment, solar, and consumer electronics industries. Dr. Hardikar has authored several technical publications and offered invited talks, including an invited paper in JMPS and an invited talk at NIST. Before joining Google, he was the Director of the Reliability Integration Simulation and Certification (RISC) group at Miasole, a global leader in CIGS PV technology.

Temporary Wafer Bonding Technology for Advanced Packaging

Thursday, 6th December
<01:50pm - 02:20pm>
Leo 2

BY

DR. **DONGSHUN BAI**
Deputy Business Development Director, Brewer Science

The current drivers for the semiconductor industry are consumer electronics, mobile devices, cloud computing, automotive electronics, 5G technology, and Artificial Intelligence. While the semiconductor industry continues to make progress in scaling integrated circuits, it is also turning to advanced packaging technologies to increase performance and integration while lowering costs. The advanced packaging landscape is changing at an astonishing speed, and the demand for faster, smaller, lower-cost devices with reduced power consumption is now greater than ever. Brewer Science was one of the first companies to consider temporary wafer bonding as an enabling technology for ultrathin wafer handling. More than ten years ago, we recognized that thin substrate handling is a fundamental processing need that cuts across many forms of advanced packaging. Nowadays, temporary bonding is not only used for wafer thinning and backside wafer processing at high temperatures and high vacuum levels, but also enables the handling of new types of packaging substrates such as reconstituted wafers and panels that easily deform under thermal stress.

To satisfy the wide range of processing requirements for different substrate types, more features must be considered in the design of temporary bonding materials. It is impractical, if not impossible, to cover the entire range of market needs with one material set or type. We have adopted a portfolio approach to material development and we utilize many different platforms to address the needs of this fast-paced market. After over 10 years of development, we have an extensive portfolio of temporary bonding materials that are compatible with all common modes of debonding, including chemical, slide, mechanical, and laser release. We are also developing new materials such as permanent adhesives, laser ablative dielectrics, and others for leading-edge packaging applications.

The presentation will illustrate the requirement and challenges for the carrier-assist substrate handling technology and introduce the advancements in the area of materials and processes that enable advanced packaging schemes such as fan-out packaging, system in package, and 3D/2.5D technology technologies. A novel dual-layer platform will also be introduced. The dual-layer system was developed to aid thin wafer handling (TWH) processes within multiple market segments including: III-V compound semi, power, 3DIC, memory, eWLB, MEMS and other FOWLP segments – all of which have stringent requirements with respect to adhesion, low total thickness variation (TTV), temperature stability, performance and form factor.

The dual-layer platform includes two layers: a thermoplastic layer and a curable layer that can be either UV- or thermally cured depending on the application. The thermoplastic layer is a conformal adhesive layer applied to the device that protects the device structures. This soluble thermoplastic layer has high glass transition temperature (Tg) and little to no melt flow at high temperature. The curable layer is applied on the carrier. It exhibits high melt flow prior to curing to enable low-temperature bonding and no melt flow after curing. Together, the two layers, which do not intermix or react chemically, enable mechanical stability and provide thermal stability up to 400°C. This system can be used with either mechanical or laser debonding methods. Other advantages of the dual-layer system include increased throughput and easy to clean after processing.

DONGSHUN BAI earned his Ph.D. in Chemical Engineering from Vanderbilt University. In 2007, he joined Brewer Science, Inc., where he has worked as Senior Scientist and Senior Program Manager in the Advanced Technologies R&D group and led the R&D work on temporary bonding and release materials. He is currently the Deputy Business Development Director of the Wafer-Level Packaging Materials business unit at Brewer Science.

Technology Trends for Large Area Panel Level Packaging

Thursday, 6th December
<01:50pm - 02:20pm>
Leo 3

BY **DR. TANJA BRAUN**
Group Lead of Assembly & Encapsulation Technologies, Fraunhofer IZM

Panel Level packaging (PLP) is one of the latest packaging trends in microelectronics. Besides technology developments towards heterogeneous integration also larger substrates formats are targeted. Fan-out Wafer Level manufacturing is currently done on wafer level up to 12"/300 mm and 330 mm respectively. For higher productivity and therewith lower costs larger form factors are introduced. Instead of following the wafer level roadmaps to 450 mm, panel level packaging might be the next big step. Easy upscaling of technology when moving from wafer to panel level as well as simple use or adaptation of existing large area tools and materials as e.g. from Printed Circuit Board (PCB) or Liquid Crystal Display (LCD) manufacturing is not possible. Additionally the missing standardization in sizes is another challenges. Considered panel dimensions ranges from 300x300 mm^2 to 457x610 mm^3 or 510x515 mm^2 up to 600x600 mm^2 or even larger.

When moving from wafer to panel level materials, equipment and processes have to be further developed or at least adapted. A view along the process chain offers lots of possibilities but also challenges. Starting from carrier material selection for a chip first approach where not only the thermo-mechanical behavior but also properties as e.g. weight or stability should be considered. Pick and place assembly on carrier is independent from wafer or panel formats a bottleneck. Here new equipment or even new approaches for high speed but also high accuracy assembly are required. Compression molding is typically used for chip embedding and to form the reconfigured wafer or panel. Liquid, granular and sheet type molding compounds are available. All allowing chip embedding with pros and cons in cost, process ability but also in cleanroom compatibility. For redistribution layer (RDL) formation a large variety of lithography tools and dielectric material options exist. As dielectrics photosensitive as well as non-photosensitive or liquid versus dry-film materials can be considered. Mask-based lithography as e.g. stepper technology is just as maskless based tools as laser direct imaging (LDI) available for panel sizes. Both offering different capabilities and strategies to overcome challenges from die placement accuracy and die shift after molding. Finally also solutions for grinding, balling and singulation are needed. Handling and especially automated handling of molded large panels including also storage and transport is still an open topic as until now only custom-made solutions exist.

However, in addition to the technical challenges also the question where is the sweet spot for large area panel level packaging is not fully answered. Here cost modelling can help to better understand overall cost structure and process and equipment assembly related to different application scenarios.

TANJA BRAUN studied mechanical engineering at Technical University of Berlin with a focus on polymers and micro systems and joined Fraunhofer IZM in 1999. Since 2000 she is working with the group Assembly & Encapsulation Technologies and since 2016 she is head of this group. Her field of research is process development of assembly and encapsulation processes, the qualification of these processes using both non-destructive and destructive tools and advanced polymer analysis. Recent research is focused on wafer and panel level packaging technologies and Tanja Braun is leading the Fan-out Panel Level Packaging Consortium at Fraunhofer IZM Berlin. In 2013 she received her Dr. degree from the Technical University of Berlin for the work focusing on humidity diffusion through particle-filled epoxy resins. Results of her research concerning packaging for advanced packages have been presented at multiple international conferences. Tanja Braun holds also several patents in the field of advanced packaging. In 2014 she received the Fraunhofer IZM research award.

ESD, EOS and AMR

Thursday, 6th December
<01:50pm - 02:20pm>
Leo 4

BY DR. **STEVAN HUNTER**
Reliability Engineering Consultant,
ON Semiconductor

Semiconductor product and IC suppliers take great care to control static voltages and discharges, ESD, and any form of electrical overstress (EOS) during manufacture and shipping, in order to ensure that each part arrives to the customer with its full reliability. Yet a high percentage of customer returns claiming unreliability has electrically induced physical damage (EIPD), indicating that ESD or EOS events occurred after the parts were out of the supplier's hands. Increased awareness and control of ESD and EOS is needed in the whole electronics industry, not just with semiconductor suppliers.

ESD is actually just one category of electrical overstress (EOS). ESD is considered as an unpowered category of EOS. EOS damage that is not ESD can also be caused in powered handling such as "hot plugging" and "switching", whether the victim parts are single or in an assembly, module or system. Control of electrostatic discharge (ESD) events is important because semiconductor devices can be physically damaged, causing failure and yield loss for the supplier. Or worse, ESD damage could be "latent", not activating until some unpredictable time later, causing an "unreliability failure" for a customer. CMOS products are especially sensitive to electrostatic discharge, but actually any electronic part can be damaged if the ESD event is severe enough. Each semiconductor product is tested for ESD tolerance as part of the product qualification, with modern IC's typically being designed to withstand greater than 1000V. Semiconductor customers must be just as careful as suppliers in controlling ESD. Even when ESD-sensitive parts are already be attached to a board, damaging ESD discharges can still occur, such as Charged Board Event and Cable Discharge Event.

Semiconductor suppliers also carefully control voltage levels during testing, to prevent electrical overstress (EOS). This includes reliability stress testing. The supplier may actually test or stress parts for short times at voltages higher than the published operating voltage for their own purposes, including burn-in or other stresses that can reveal the presence of defects. Of course any parts with weaknesses detected are either repaired or scrapped. Certain product quality reliability stress tests include higher voltage and other stresses, to "accelerate" the weakest failure mechanisms. A successful product qualification indicates that those batches of parts from manufacturing are sufficiently reliable to perform for the full warranty period. Reliability stress testing is considered destructive testing, and these parts are not shipped.

Determination of operating conditions and the Absolute Maximum Ratings (AMRs) are the responsibility of suppliers. AMRs may be listed on the data sheet, specifying to customers to never allow stresses to exceed these known limits. A customer may choose to operate the product slightly above the operating conditions for short times, realizing that reliable lifetime is being compromised. But parts stressed beyond AMR limits may become unpredictably unreliable. Additional failure mechanisms may become active. Permanent alteration in the materials occur. It is the customer's responsibility to preserve the product reliability by operating within the specified limits, and especially to never allow stress to exceed AMR limits. Methods for AMR determination are not consistent among suppliers, and interpretation of AMRs by customers vary widely. The ESD Association is currently conducting research, intended to aid both suppliers and customers in determination, specification and interpretation of AMRs for best success in reliable product use.

STEVAN HUNTER ,PhD, is Reliability Engineering Consultant and ESD Control Champion at ON Semiconductor in Phoenix, Arizona, USA, with 40 years of experience in Semiconductor engineering. He also manages university research projects for ON, and teaches as Faculty Associate at ASU, BYU-Idaho and UMD CALCE.

TSV interconnect based 3D/2.5D IC packaging technology and market trends

Friday, 7th December
<08:30am - 09:00am>
Gemini 2

BY

MR. **SANTOSH KUMAR**
Director & Principal Analyst,
Yole Développement

TSV interconnect based 3D/2.5D packaging has gained significant attention since its introduction in FPGA (for die partitioning) and HBM integrated GPU module (for gaming application). The performance potential offered by this technology is unequalled by any other packaging platform today. High-end applications like deep learning, datacenter networking, AR/VR, and autonomous driving are becoming real, thereby pushing the limits of other current packaging platforms. Fueled by increasing bandwidth needs for moving data in cloud-computing and supercomputing applications, performance-driven markets have adopted 3D stacked technologies in a row. Imaging, as the first market adopter of 3D integration, is propelling the market with an increasing number of sensors in smartphones and tablets, including 3D imaging. TSV-based products can be classified in three ranges: low, middle, and high-end. The middle and high-end product markets like CMOS image sensor, memory cube, and interposer are based on a via-middle process. In low-end products, we can also find TSV based on via-middle (i.e. in Apple's fingerprint sensor), but for cost reasons the MEMS industry is using essentially a via-last process, which is cheaper than a via-middle process. TSV's penetration rate in low-end products will remain stable, with the main source of growth due to RF filters in smartphone front-end modules, which keep increasing in order to support the different frequency bands used in 5G mobile communications protocol. This presentation will discuss about the market and technology trends of the TSV based 3D/2.5D packaging.

SANTOSH KUMAR is currently working as Director & Principal Analyst at Yole Développement. He is involved in the market, technology and strategic analysis of the microelectronic assembly and packaging technologies. His main interest areas are advanced IC packaging technology including equipment & materials. He is the author of several reports on fan-out / fan-in WLP, flip chip, and 3D/2.5D packaging.

He received the bachelor and master degree in engineering from the Indian Institute of Technology (IIT), Roorkee and University of Seoul respectively. He has published more than 40 papers in peer reviewed journals and has obtained 2 patents. He has presented and given talks at numerous conferences and technical symposiums related to advanced microelectronics packaging.

Engineering Green Electronics

Friday, 7th December
<08:30am - 09:00am>
Leo 1

BY **PROF. DAVID MARK HARVEY**
Electronic Engineering at Liverpool
John Moores University

The ubiquitous nature of electronics in daily life coupled with the Moore's Law type enhancements in the integrated circuit field now requires serious thinking about how to "green" electronics technology.

Packaging, circuit interconnections and size will keep getting smaller but how far can we move to green-up the business? Design for manufacture, test, reliability, EMC and low power are important considerations, but have we considered how to use more environmentally friendly components and at the end of life methods to reduce landfill through more efficient recycling.

Key to less wastage are more reliable products, and some recent work completed on through-lifetime monitoring of solder interconnections on area array packages will be considered. Lifetime testing of area array packages through both thermal cycling and vibration has started to identify failure mechanisms by imaging the hidden solder balls. Extensive ultrasound scans and some X-ray imaging have helped measure the failure progression from new product to failure.

Failure mechanisms in manufactured electronics are often caused by mismatches in the individual coefficients of thermal extension, differences in stiffness/rigidity, and poor component placement. Can new materials be invented at an appropriate cost to better match up the individual design components and reduce failure/stresses for increased lifetime and more reliable products? If these new materials can also be environmentally friendly and easily recyclable then we have gone some way towards green electronics.

Work completed has started to find failure profiles for lead-free solder joints and examples will be given on real test samples for area array packages lifetime tests and embedded die delamination failure analysis. In future new types of solder will be important and further work on new materials is required here. Some joint work has recently started on design and lifetime analysis new solder materials between Malaysia and the UK through a two-year Newton project.

An important aspect of measuring hidden solder joints or die is to separate the layers to find the exact position of any fault that may occur during lifetime tests. The team have designed an image processing toolbox that can separate overlapped layers in ultrasound scans such that a type of "Data Fracking" using complex wavelets can isolate the depth of previously undetectable faults. So turning a series of 2D horizontal scans into a 3D layered picture.

DAVID MARK HARVEY is Professor of Electronic Engineering at Liverpool John Moores University. UK. He conducts research, teaching and enterprise work in digital electronics design, manufacture and test. He has published over 100 articles and successfully supervised 17 PhD students. He has directed two large technology transfer projects funded to €10M, and through these projects worked with over 250 companies. All research work has an industrial bias and the graduates produced have entered industry in the electronics sector. Of three recent PhD graduates, one is European validation manager for a large multinational automotive electronics company, one is working in product validation at Intel in Penang, and a third entered Cambridge Silicon Radio (now Qualcomm). In the past he has helped set up two design centres in India, and worked for companies in the UK in the steel industry, high vacuum scientific instruments and secure electronic communication. His present interests are in the design, manufacture and test of automotive and space electronics.

Organic substrate material with low transmission loss and effective in suppressing package warpage for 5G application

Friday, 7th December
<08:30am - 09:00am>
Leo 2

BY MR. SHUNSUKE TONOUCHI
Laminate Material R&D Dept.,
Hitachi Chemical Co., Ltd

Mobile communication system has been graded up in every decade. The next generation system, which is called 5G, is coming. The data transmission speed of mobile device will be 10 Gbps or higher. Such a high performance infrastructure can change the world and strongly support autonomous, IoT/IoE and other emerging systems. The frequency band used in 5G is now discussing in the standardizing organizations and each government. Some bands of millimeter wave between 20 to 80 GHz are strong candidates. Signal transmission loss is proportional to transferring frequency, and dielectric dissipation factor (Df) and a root of dielectric constant (Dk) of dielectric constant. Dielectric material with low Dk and Df is preferably required for high frequency signal transferring system. The low loss system can suppress the power consumption and heat generation. Thinner form factor is kept demanded in the package of mobile device like smart phone and tablet. Substrate is also required to be thin with the performance of suppressing the package warpage in such an application. Therefore, the package substrate for 5G mobile device will be required to satisfy the low transmission loss and the small package warpage. Low coefficient of thermal expansion (CTE) is known for reducing package warpage, so the substrate material with low CTE is also required. Additionally, other than the package substrate such performance material is also expected for the mother board of mobile device

In this research the substrate material having low Dk and Df, and CTE has been developed. The material is the composite of the originally designed thermosetting resin and the glass fabric. The base resin system is composed of the hard and the soft segment. The former segment consisted of the polycyclic resin having the planer stack structure of aromatic ring. The strong intermolecular force between the stacks restricts the local movement of the resin system, which can contribute to the small CTE and the low Df. The latter segment can make the resin component follow the thermal behavior of the glass fabric which is a small CTE material. Consequently, the composite material can show the very small CTE which is close to that of the glass fabric. Moreover, the low elastic modulus of the resin system, which is derived from the latter segment, works well to lower the residual stress. It is effective in the package warpage suppression. Using low or non polarity component is a basic idea to design low Dk and Df resin system. The hard segment of polycyclic resin has some polarity. In general different polarity components have less compatibility each other. We have overcome the compatibility issue by introducing chemical co-crosslinking reaction modifying both the polycyclic and the low polarity components. Tg, CTE, Dk and Df of the developed composite material are 220 degree C, 6.0 ppm/degree C, 3.5 to 3.6 (@ 10 to 77 GHz) and 0.0035 to 0.0065 (@ 10 to 77GHz), respectively. Tg and CTE were evaluated by thermos mechanical analysis. Dk and Df were measured by triplate resonator method for 10 GHz and cut-off circular waveguide method for 77 GHz. Warpage behavior of the package was evaluated comparing with the conventional coreless thin substrate. The package and the die size were 14 x 14 and 7.3 x 7.3 mm2, respectively. The substrate was 300 um thick and 5 layer coreless structure. Convex warpage was observed at the cooling step after reflow. The warpage value was 150 um. It was smaller than that of the conventional substrate, which was 167 um. Signal transmission property at 28 to 77 GHz was also evaluated by making Cu micro strip line on the substrate. The loss values at 28 and 77 GHz were 0.47 and 1.38 dB/cm, respectively. Those were smaller than the values of the conventional one, which were 0.87 and 2.30 dB/cm, respectively. Better performance of the developed material regarding signal transfer and warpage suppression was clearly shown. And an insulation reliability evaluation of bias-HAST. 12 Volt bias was applied to the comb electrode of line and space of 30 and 30 um, which was formed on the material. No electrical insulation degradation was observed at 130 degree C and 85%RH for 200 hours

SHUNSUKE TONOUCHI is currently in Laminate Material R&D Dept., R&D Headquarters, Hitachi Chemical Co., Ltd. He holds Master degree in environmental studies from Tohoku University, Miyagi, Japan, in 2013 after getting Bachelor degree in engineering from Tohoku University, Miyagi, Japan, in 2011. His main study was nanoscience of inorganic chemistry. He has been working in the field of resin design and polymer synthesis for organic substrate material since then.

Electronic Materials and Packaging Trends in the Era of Digital Transformation

Friday, 7th December
<08:30am - 09:00am>
Leo 3

BY MS. **ROZALIA BEICA**
Global Director Strategic Marketing, Electronics & Imaging, Specialty Products Division, DowDuPont

Digital transformation is further expanding into new markets bringing new application opportunities and driving increased adoption of electronics and semiconductor devices. The explosion of new applications is driving the semiconductor industry to transition from a technology node to an application driven industry. While advancing the technology node continues, new architectures and integration technologies are being developed to address the increased market requirements and the need of integrating more functionalities within smaller and more compact systems. A wide range of packaging technologies have already been successfully developed and adopted in the industry enabling single and multi-die packaging. While these technologies will continue to grow and further evolve, heterogeneous integration is gaining a lot of interest in the industry due to several benefits it can bring. This will also drive the need for more performing electronic materials and processes.

The presentation will provide an overview of the major trends (5G, Artificial Intelligence, IoT, Autonomous Driving, etc.) driving the semiconductor and packaging industry. The talk will highlight the various packaging platforms and their evolution as well as the material and processing challenges and needs driven by the new applications. Examples of DowDuPont activities and materials and its commitment to future innovation, collaboration and sustainability will also be included.

ROZALIA BEICA is Global Director Strategic Marketing, Electronics & Imaging, Specialty Products Division of DowDuPont. In her current role, Rozalia leads strategic marketing activities across Electronics & Imaging Division. She has 25 years of international working experience across various industries, including industrial, electronics and semiconductors. For 19 years she was involved in the research, applications and strategic marketing of Advanced Packaging technologies, with global leading responsibilities at specialty chemicals (Rohm and Haas Electronic Materials), equipment (Semitool, Applied Materials and Lam Research) and device manufacturing (Maxim IC). Prior to joining Dow, Rozalia was the CTO of Yole Développement where she led the market research, technology and strategy consulting activities for Advanced Packaging and Semiconductor Manufacturing.

Throughout her career, Rozalia has been actively supporting industry activities worldwide: Program Director of EMC3D Consortia, General Chair of IMAPS Device Packaging and Global Semiconductor and Electronics Forums, Technical Advisory Board Member at SRC, Member of the Executive Committee of ECTC, IMAPS SiP, ISQED, ESTC and member of several committees worldwide (ITRS, IWLPC, EPTC and EPS). Current industry involvements include: IMAPS VP of Technology, Technical Chair IMAPS Advanced SiP, Executive Committee Member of SiP China, ECTC Assistant Program Chair, HIR WLP Chair, Advisory Board Member of 3DinCites and IMPACT Taiwan. She has over 150 presentations and publications (including 3 book chapters on 3D IC technologies), several keynotes, invited presentations and panel participations.

Rozalia has a M.Sc. in Chemical Engineering from Polytechnic University "Traian Vuia" (Romania), a M.Sc. in Management of Technology from KW University (USA), and a Global Executive MBA from Instituto de Empresa Business School (Spain).

Thermal and Failure Analysis of Advanced Sub-micron Devices Using Transient Thermoreflectance Thermography

Friday, 7th December
<08:30am - 09:00am>
Leo 4

BY DR. **ANDREW TAY**
Adjunct Fellow, Singapore University of Technology and Design

Thermal characterization of sub-micron devices, detecting sub-micron time-dependent thermal defects and identifying those that represent potential device failures is a challenge in the thermal analysis of today's complex electronic devices. The scaling of device features results in a significant reduction in time response and an increased sensitivity to transient events. With today's complex devices very small localized temperature 'hot spots' can occur due to an unintended functional anomaly in a circuit with a tight design margin or a timing perturbation resulting from a small change in capacitance or another parameter elsewhere in the circuit. As device features continue to shrink so do the challenges of detecting circuit-induced thermal defects. While gaining a full understanding of the device thermal behavior is getting more difficult, extremely high power densities are increasing the importance of having this understanding. Clearly just having average temperature rise information is not sufficient, it is necessary to have a clear understanding of temperature distributions with submicron resolution to detect local hotspots and nanosecond, and even picosecond, temporal resolution to observe time-dependent thermal events with today's high-speed devices.

In this presentation, an overview of the merits and demerits of various techniques for measuring device thermal behavior will be presented. Thermoreflectance thermography (TRT) will then be described in greater detail and it will be shown how it can be used to thermally analyze today's device structures using illumination wavelengths in the visible range. This imaging technique enables spatial resolution of down to 0.25 micron and when combined with temporal resolution in the nanosecond range meets the requirements necessary to fully characterize the thermal behavior of today's advanced complex device structures. Several case studies will be described.

ANDREW TAY is an Adjunct Fellow at the Singapore University of Technology and Design and a technical consultant. He is a former Professor of Mechanical Engineering at the National University of Singapore. Dr Tay obtained his B.E. (Hons I and University Medal) and PhD in Mechanical Engineering from the University of New South Wales, Australia. His research interests include electronics packaging (thermo-mechanical failures, delamination, effects of moisture, solder joint reliability, TSVs); thermal management of electronic systems and EV batteries, thermoreflectance thermography, solar photovoltaics and fracture mechanics. He is currently the IEEE EPS Director of Student Programs, a member of the EPS Board of Governors, the Chairman of the IEEE Singapore Reliability/EP/ED Joint Chapter, and Chairman of the EPTC Board. He was the inaugural General Chair of the 1st Electronics Packaging Technology Conference (EPTC) in 1997. He has served or is still serving in the International Advisory Boards and Organising committees of several regular international electronics packaging conferences such as DTIP, ECTC, EMAP, EPTC, EuroSime, HDP, ICEPT, IEMT, IMPACT, InterPack, ITHERM and THERMINIC.

For his exceptional technical achievements, he was awarded the 2012 IEEE CPMT Exceptional Technical Achievement Award, and for his contributions to IEEE CPMT Society Region 10, the 2012 IEEE CPMT Regional Contributions Award. For his outstanding contributions in the application of engineering mechanics to electronics and/or photonics packaging, he was awarded the ASME EPPD Engineering Mechanics Award in 2004. He was also awarded an IEEE Third Millennium Medal in 2000. He is a Fellow of ASME and a member of IEEE.

Novel Thin Wafer De-bonding System for 3D TSV Multi-Chip Packaging of High Bandwidth Memory Devices

Friday, 7th December
<01:30pm - 02:00pm>
Gemini 2

BY DR. **MIN WOO RHEE**
Program Manager and a Principal Engineer with the Manufacturing Technology Research and Development Center, Samsung Electronics

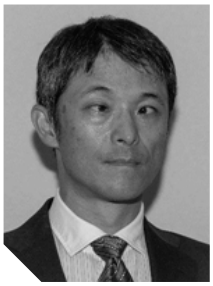
The stable temporary bonding and de-bonding system for 3D IC packaging is one of the most crucial processes to achieve successful 3D HBM memory device stacking by applying TSV (Through Silicon Via) technology. However, there are not much proven de-bonding systems with sufficient stability and reliability to handle less than 50 wafer thickness. To meet those challenges, lots of temporary bonding and de-bonding concepts have been investigated through the 3DIC integration history for both in industry and research. The concept for the first generation was the mechanical de-bonding system using thermoplastic resins which has been widely used above 100 thin wafer handling system such as thermal slide off or lift off type. However, since those de-bonding system inevitably induce huge amount of mechanical stresses on the thin downed wafer it is very difficult to establish stable process condition when the thickness requirement is move down to 50. In addition, since the de-bonding mechanism is often complicit with the material requirement during 3DIC process. It should withstand high temperature and high vacuum process such as dielectric cure and PECVD, even in chemical process. If the adhesion is strong then the reliability of the temporary bonded layer is good enough to withstand various conditions of 3DIC processes, however de-bonding process is too challenging since the adhesion between the bonded pair is already strong. On the contrary, if the adhesion of bonded pair is weak enough to provide easy de-bonding condition, then 3DIC process stability is drastically going down. To overcome those challenges, recently the scientist and researcher are more focused on different process mechanism between temporary bonding and de-bonding, such as temporary bonding by polymer crosslinking and de-bonding process by focused laser between the interfaces of bonded pair, but report has it that this method also have much concerns because it could damage the active layer on the devices. To overcome those technical challenges, the authors suggest novel damage free thin wafer de-bonding system which can apply high power UV irradiation with specific wave length on UV sensitive polymer film on glass carrier wafer. The experimental analysis shows that the developed system is able to de-bond the thin wafer from the carrier with no damage and sufficient productivity for mass production.

MIN WOO RHEE was born in Seoul, South Korea, in 1973. He received the B.Eng. (Hons.), M.Sc., and the Ph.D. degrees in chemical engineering from Sogang University, Seoul, and the master's degree in management of technology from National University of Singapore (NUS), Singapore. He has about 20 years' experience in microelectronics packaging research and development for both industry and research institutes. He also has extensive experience in advanced packaging and material development, modeling and characterization. He was also with Amkor Technology Research and Development from 1999 to 2010, where he was the Senior Manager and the Leader of the Material Characterization Modeling and Failure Analysis Group. He also resolved lots of chronic failure and quality issues with the worldwide semiconductor companies. He is currently working as the Program Manager and a Principal Engineer with the Manufacturing Technology Research and Development Center, Samsung Electronics, Hwasung, South Korea. Before his joining Samsung Electronics, he was a Scientist and the Group Leader in interconnection and advanced packaging program (IPP) with the Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR), Singapore. During his working periods in IME A*STAR from 2011 to 2015, he led power module, ruggedized electronics research groups, and industry consortium projects for automotive, oil and gas, deep sea exploration, and aerospace industries. He also has project leading experience on lots of public funded and industry projects related to material and advanced packaging development, such as MEMs, 3-D-IC and fan-out wafer level packaging. In addition, he had developed an automotive three-phase inverter module for power electronics with the Fairchild Semiconductor Research and Development Group as a Principal Engineer, which were successfully implemented for mass production in major automotive industries. He is the author and co-author of 65 journals and conference papers and has more than 20 patents related with microelectronics and advanced packaging area. Also he is the winner of "the Future Creator Award" from Samsung Electronics in 2018 and the "Best Employee of the Year" Award when he was with Amkor in 2009.

Low temperature interconnect technology using Sn-Bi alloy system for high performance packages

Friday, 7th December
<01:30pm - 02:00pm>
Leo 1

BY MR. KEI MURAYAMA
R&D in Packaging, SHINKO



Recent years, a low temperature interconnection using Sn-Bi solder has received remarkable attention from semiconductor packaging and SMT industry. Because high temperature warpage induces reducing yield during solder reflow. And in case of large size die application, CTE mismatch between a silicon die and an organic substrate induce large stress at solder interconnection. In addition, electro-migration phenomenon is the most significant problem for high performance packages. The current density at the micro solder joint is expected to be in the order of 10kA/cm2. In case of Sn3.0wt.%Ag0.5wt.%Cu (SAC) solder which is conventional lead-free solder, large cracks are formed at the cathode interface after current stressing. On the other hand, in case of Sn-Bi solder, vacancy or crack is not formed at the cathode interface even after long time current stressing. Sn-Bi solder is strong candidate materials to improve package reliability.

Firstly, we introduce the difference of warpage behavior and stress change between Sn 57 wt.% Bi (Sn57Bi) solder and SAC solder in the flip chip interconnection area using a large die (20 × 20 mm). The reflow peak temperature of Sn57Bi solder and that of SAC solder were 180 degrees C. and 245 degrees C., respectively. The warpage after chip mounting using Sn57Bi solder and that of using SAC solder were 36.0 μm and 96.5 μm, respectively. And microstructure and strain analyses of the flip chip interconnection area were performed on both Sn57Bi and SAC solder by Electron backscattered diffraction (EBSD). Regarding initial state of SAC solder, at the corner bump, the average grain size of -Sn was 28.8 μm. After thermal cycling (TC) test, the average grain size of -Sn was refined less than 6 μm. Regarding Sn57Bi solder, at the initial state, the average grain size of -Sn at all location was less than 4.4 μm. After Thermal cycling (TC) test, the average grain size of -Sn was less than 4.5 μm. Refining of -Sn was hardly observed. We employed Grain Reference Orientation Deviation (GROD) analysis for strain analysis. As the plastic strain increases, the GROD value increases. In the case of initial state of SAC solder, high angles were observed at the corner bump and strain concentration were observed at the edge of Cu pillar and at the edge of substrate pad. After TC test, crack propagation was observed at the same point. On the other hand, in the case of Sn57Bi solder, high angles were less than 3 % and strain concentration were not observed. After TC test, crack propagation was not observed. These results suggest that using Sn57Bi solder is less affected by thermal stress than using SAC solder. Secondly, we introduce the difference of electro-migration mechanism between SAC and Sn-Bi solder. The current density was 40KA/cm2 and test temperature were 150 degrees C.(SAC) and 125 degrees C.(Sn-Bi), respectively. In the case of SAC solder, the resistance change was hardly observed at 100 hours. But the resistance rapidly has increased and the electrically open failure was observed at 140 hours. Sn atoms migrated to the anode side by the electron flow but the metal atoms hardly move by the back flow. Crack were formed at the cathode interface. On the other hand, Sn57Bi solder showed the behavior that was different from SAC solder. The resistance had gradually increased to 25 % at 100 hours. And after, the resistance had gently increased to 80 % at 3300 hours. Bi atoms migrated to the anode side and accumulated on Cu pillar by the electron flow. And Sn atoms migrated to the cathode side by the back flow. However, vacancy or crack was not formed at the cathode interface. Because resistivity of Bi is higher than Sn, resistivity change of Sn-Bi system was affected by Bi content. In the case of Sn30wt.%Bi(Sn30Bi), the resistance change was less than 20% at 2000 hours. Sn30Bi solder showed high electro-migration resistivity. We also introduce 2.5D application using Sn-Bi solder. Sn-Bi solder has employed for interconnection between an interposer and an organic substrate. We found that using Sn-Bi solder can reduce the warpage and the solder interconnection stress

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KEI MURAYAMA received his B.E. and M.E. degrees in chemical engineering from Shinshu University, Nagano, Japan in 1991 and 1993, respectively. He joined SHINKO ELECTRIC INDUSTRIES CO., LTD. in 1993. He has been engaged in the research and development of semiconductor packaging. He has 25 years of experience in semiconductor packaging industry and has worked in various interconnect techniques and packaging techniques such as solder ball formation, flip chip bonding, TLP bonding, silicon package, silicon interposer, wafer bonding and HS attach. His current research interests include a low temperature and a low stress bonding for high performance package such as organic interposer. He is mainly working on the development of flip chip bonding technique using low temperature solder and elucidation of its electro-migration phenomenon. And his current interests also include microstructure and crystal orientation analyses of the interconnection bump by Electron probe micro analyzer (EPMA) and Electron backscattered diffraction (EBSD).

Effects of Aging on the Reliability of Electronic Products Incorporating Lead Free Solders

Friday, 7th December
<01:30pm - 02:00pm>
Leo 2

BY **PROF. JEFFREY C. SUHLING**
Quina Distinguished Professor and Department Chair
of Mechanical Engineering at Auburn University

Environmental concerns and legislation adopted in Europe and Asia has led to a nearly universal world-wide transition to lead free solders (so-called SAC alloys) in electronic products over the past 15 years. One of the greatest challenges has been that lead free solders are highly susceptible to aging effects, where their mechanical behavior and failure properties degrade with time when exposed to isothermal or variable temperature environments. Such degradations are caused by the unstable microstructures present at very low temperatures, and they can lead to a significant reduction in the reliability of electronic products with time.

In this talk, an overview of our research on the effects of aging on the mechanical behavior of lead free solders is presented. This work as involved a combination of experimental material characterization and measurements of microstructural evolution, as well as constitutive model development and finite element predictions of reliability. Stress-strain and creep tests have been performed using miniature tensile samples, and the degradations in the effective elastic modulus, yield stress, ultimate tensile strength, and creep strain rate have been characterized and modeled as a function of aging temperature, aging time, and alloy composition. Analogous results have also been obtained using nanoindentation testing of small solder joints from non-aged and aged lead free electronic assemblies. Finally, cyclic stress-strain testing has been utilized to understand the aging induced degradations in the hysteresis loop and fatigue life. The results of the experimental mechanical testing have been correlated with observations of microstructural evolution occurring in lead free solders during aging to develop a fundamental understanding of the causes of the material property degradations. In addition, methods to mitigate aging effects have been developed through the use of microalloy additions. Finally, the measured data have been used to build aging effects into the Anand viscoplastic constitutive model as well as a modified Morrow model for fatigue life, and then implemented in finite element simulations to make reliability predictions for electronic products subjected to aging.

JEFFREY C. SUHLING received his Ph.D. degree in Engineering Mechanics in 1985 from the University of Wisconsin. He then joined the Department of Mechanical Engineering at Auburn University, where he currently holds the rank of Quina Distinguished Professor and Department Chair. From 2002-2008, he served as Center Director for the NSF Center for Advance Vehicle Electronics. His research interests include solid mechanics, stress and strain analysis, material characterization, experimental mechanics, advanced and composite materials, finite element analysis and computational mechanics, additive manufacturing, electronic packaging, and silicon sensors. Dr. Suhling has authored or co-authored over 400 technical publications, and he has advised over 80 graduate students at Auburn University. He is a Fellow of ASME, and is a member of IEEE, SMTA, IMAPS, SEM, and TAPPI. He served as Chair of the Electrical and Electronic Packaging Division of ASME during 2002-2003, and was on the EPPD Executive Committee from 1998-2003. Dr. Suhling was the Technical Program Chair of the ASME InterPACK '07 Conference, and General Chair of the ASME InterPACK '09 Conference. He currently serves on the IEEE Electronics Packaging Society Board of Governors, and is the General Chair of the 2019 IEEE ITherm Conference

Package Level Systems Integration: A key to maintaining the pace of progress

Friday, 7th December
<01:30pm - 02:00pm>
Leo 3

BY DR. **BILL BOTTOMS**
Chairman of Third Millennium Test Solutions

The most efficient path for progress in electronic systems for more than 50 years has been Moore's Law scaling but the advantages of scaling CMOS are now approaching their economic end. Information technology must identify new approaches if the economic and societal benefits are to maintain their pace of progress in the post Moore's Law era. This need has accelerated innovation in new technologies to maintain the improvements in size, cost, performance and power efficiency that has driven information technology into every corner of human activity over the last 50 years. The coming changes are evident with evolutionary progress in advanced packaging, introduction of new system architectures, new device types, new materials and new processes for both design and production. The evolution includes wafer level packaging, 3D integration and heterogeneous integration of known components into a single package.

The revolution that is just beginning will include a complete remake of the global network, new devices for both logic and memory functions, an array of sensors of all types. The emergence of big data, the internet of things and migration of memory, logic and applications to the cloud are moving the majority of power usage from logic towards memory transport. The path toward maintaining the pace of progress for decades to come will, however, transform this evolution in the industry to an industrial revolution where new device types and other components are integrated into systems at the package level. The ultimate realization of this revolution will be full system integration of complex products in the package. There are difficult challenges that must be overcome to realize this revolution. Many of the elements of this revolution are in development today and will be discussed in this presentation.

BILL BOTTOMS received a B.S. degree in Physics from Huntington College in Montgomery, Alabama in 1965, and a Ph.D in Solid State from Tulane University in New Orleans in 1969 and is currently Chairman of Third Millennium Test Solutions. He has worked as a faculty member in the department of electrical engineering at Princeton University, manager of Research and Development at Varian Associates, founding President of the Semiconductor Equipment Group of Varian Associates and general Partner of Patricof & Co. Ventures.

Dr. Bottoms has participated in the start-up and growth of many companies through his venture capital activity and through his own work as an entrepreneur.

He has served as Chairman and CEO of many companies both public and currently serves as: Emeritus Member of the Board of Tulane University, Co-Chair of the Heterogeneous Integration Roadmap, Chairman of the SEMI's Awards Committee, Chairman of the Packaging and Package Substrates Technical Working Group for INEMI, Member of the Board of MIT's Microphotonic Center, Chairman of Fluence Analytics, Chairman of Third Millennium Test Solutions.

LED multiphysics modelling for “Industry 4.0”, an approach proposed by the Delphi4LED European project

Friday, 7th December
<01:30pm - 02:00pm>
Leo 4

BY PROF. MÁRTA RENCZ
Budapest University of Technology and Economics

The Delph4Led project of the European Union is targeting paradigm shift in lighting design. The Industry 4.0 initiative targets the digitalization of design and manufacturing processes. In line with this initiative the aim of the Delphi4LED project is to trigger this transition in the solid-state lighting industry by enabling digital design of LED based systems, e.g. luminaires. As LEDs are strongly multi-physics devices, producing light, controlled electronically, depending very strongly on temperature, their characterization is a very complex task. For the description of the operation complex testing and modeling methodologies have to be developed, optimized and standardized.

In our paper we first present the Industry 4.0 concept and its specialties in solid state lighting (SSL) system design. We introduce the X diagram to demonstrate the various aspects and levels of designing an SSL system. We present how the digital twin concept appears on package and luminaire level.

We present the workflow proposed by the Delphi4LED consortium, starting from the standardized measurements of the LED devices, followed by standardized test data reporting, and LED device modeling. The physics based compact modeling approach is presented in details. The LED package characterization enables LED package multiphysics modelling as well, that together with LED model will serve as the input of system level multi domain modeling of LED based systems. These models can be simulated together with the 3D multiphysics model or the compact thermal model of the luminaire, to enable virtual prototyping of solid state lighting systems, for fully digitized lighting design, considering all the electrical and thermal boundary conditions.

The paper present how to obtain the digital twin of an LED device and the digital twin of an LED package and that of a luminaire, and present how these digital twins can be connected to enable simulation of the whole system. This simulation is extremely fast and enables design optimizations such a determining the number of LEDs, the required luminaire thermal resistance, the forward current etc. so as to achieve required luminous flux, keep within total power dissipation constraints and limit operating temperatures.

In the presentation both the testing and modeling approaches will be presented with examples. The digital twin based lighting design will be shown with a simulation example. The standardization approaches will also briefly discussed.

MÁRTA RENCZ received the electrical engineering degree and the Ph.D. degree from the Technical University of Budapest, Hungary. She is a professor at the Budapest University of Technology and Economics.

She was a co-founder and CEO of Micred Ltd that is now part of Mentor, a Siemens business, where she still holds a research director position. She has participated in numerous international research projects, mostly in the field of investigating, measuring and modeling multi-physical effects in electronics. She has published her theoretical and practical results in more than 300 technical papers. She holds various awards of excellence, among others the Allan Krauss thermal management award of ASME.

Technical Session A

Thursday, 6th December
<09:00am - 10:00am>

Technical Session S-01: Advanced Packaging I	
Chair: Dr. Beth Keser	Room: Gemini 2
A-01 **ID:246** 09:00am	**Innovative Packaging Solutions of 3D System in Package with Antenna Integration for IoT and 5G Application** Author(s) - Mike Tsai, Ryan Chiu, Eric He, J.Y. Chen, Royal Chen, Jensen Tsai, Yu-Po Wang *SPIL, Taiwan | miketsai@spil.com.tw*
A-06 **ID:176** 09:20am	**Concepts for a Monostatic Radar Transceiver Front-end in eWLB Package with Off-Chip Quasi-Circulator for 60 GHz** Author(s) - Philipp Schmidbauer[1], Maciej Wojnowski[2], Robert Weigel[1], Amelie Hagelauer[1] *[1]Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany* *[2]Infineon Technologies AG* *philipp.schmidbauer@fau.de*
A-11 **ID:141** 09:40am	**Ceramic Interposers for Ultra-High Density Packaging and 3D Circuit Integration** Author(s) - Arash Adibi, Aria Isapour, Ammar Kouki *École de technologie supérieure, Canada | arash.adibi@lacime.etsmtl.ca*

Technical Session S-02: Interconnect Technologies I	
Chair: Prof. Sarah Kim	Room: Leo 1
A-02 **ID: 284** 09:00am	**Estimation of Maximum Operating Temperature for Cu Wire Bonds: Comparison of Epoxy and Silicone Encapsulant Types** Author(s) - Stevan G Hunter[1], Michael Hook[2], Michael Mayer[2] *[1]ON Semiconductor, United States of America [2]University of Waterloo, Canada* *sputterman0@gmail.com*
A-07 **ID: 247** 09:20am	**High strength bonding on ENIG surface with microporous Ag sintering under a low temperature pressureless condition** Author(s) - Zheng Zhang, Chuantong Chen, Katsuaki Suganuma *Institute of Scientific and Industrial Research, Osaka university, Japan |* *hangzheng@eco.sanken.osaka-u.ac.jp*
A-12 **ID: 285** 09:40am	**Cu Sinter Pastes for Pure-Cu Die-Attach Applications of Power Modules** Author(s) - Barbara Eichinger[1,2], Martin Mischitz[1], Susan Ohm[1,3], Torge Behrendt[4], Fabian Craes[4], Roland Brunner[5] *[1]Infineon Technologies Austria AG, Austria* *[2]Department of Physics, University of Graz, Graz, Austria* *[3]RWTH Aachen, Aachen, Germany* *[4]Infineon Technologies AG Warstein, Germany* *[5]Materials for Microelectronics, Material Center Leoben, Leoben, Austria* *barbara.eichinger@infineon.com*

Technical Session S-03: Materials and Processing I		
Chair: Prof. Klaus-Dieter Lang		Room: Leo 2
A-03 **ID: 241** 09:00am	**Suitable Cu leadframe material and design to achieve high reliability requirement and good manufacturability** Author(s) - Jun[leo] Li, Lidong Zhang, Allen Descartin, Jinmei Liu *NXP Semiconductors, China, People's Republic of | Leo.l@nxp.com*	
A-08 **ID: 205** 09:20am	**Package Integrity and Reliability Effects of Mold Compound Chemistry For Power Device Application** Author(s) - Matthew M. Fernandez[1], April Joy H. Garete[2], Reinald John S. Roscain[2] *[1]Department of Mining, Metallurgical and Materials Engineering, University of the Philippines - Diliman;* *[2]Nexperia Philippines, Inc., Philippines* *april.joy.garete@nexperia.com*	
A-13 **ID: 175** 09:40am	**Thermomechanical and Viscoelastic Properties of Dielectric Materials Used in Fan-Out Wafer-Level Packaging** Author(s) - Yosephine Andriani[1], Xiaobai Wang[1], Songlin Liu[1], Zhaohui Chen[2], Xiaowu Zhang[2] *[1]Institute of Materials Research and Engineering, Singapore* *[2]Institute of Microelectronics, Singapore* *andrianiy@imre.a-star.edu.sg*	

Technical Session S-04: Emerging Technologies I		
Chair: Ms.Rozalia Beica		Room: Leo 3
A-04 **ID: 127** 09:00am	**Pluggable Silicon Photonics MEMS Switch Package for Data Centre** Author(s) - How Yuan Hwang *Tyndall National Institute, Ireland* *howyuan.hwang@tyndall.ie*	
A-09 **ID: 206** 09:20am	**Post processing of a SiN-based photonic stack above a CMOS imager sensor** Author(s) - Nga Phuong Pham, Bert Du Bois, Rita Van Hoof, Gillis Winderickx, Hemant K. Tyagi, Deniz Sabuncuoglu, Harrie A.C. Tilmans *imec, Belgium* *pham@imec.be*	
A-14 **ID: 326** 09:40am	**Evaluation of Piezoresistive Polymer-based Traces for Non-invasive Sensor Patch** Author(s) - Maria Ramona Ninfa B. Damalerio, Ruiqi Lim, Weiguo Chen, David Sze Wai Choong, Ming-Yuan Cheng *Institute of Microelectronics, A-STAR, Singapore* *david_choong@ime.a-star.edu.sg*	

Technical Session S-05: Thermal Characterization & Cooling Solutions I

Chair: Mr. Rathin Mandal — Room: Leo 4

A-05
ID: 305
09:00am

Extending the Cooling Limit of Automotive Camera Advanced Driver Assistance Based on Usage Conditions

Author(s) - Hoa Do, Gamal Refai-Ahmed
Xilinx Inc., United States of America
hoa.do@xilinx.com

A-10
ID: 113
09:20am

Thermal simulation and measurement of components in avionics

Author(s) - Jung Kyun Kim[1], Su Heon Jeong[2]
[1]Mentor, a Siemens Business, Korea, Republic of (South Korea)
[2]Defense Agency for Technology and Quality
jeff_kim@mentor.com

A-15
ID: 126
09:40am

Si-based Hybrid Microfluidic Cooling for Server Processor of Data Centre

Author(s) - Yong Han, Boon Long Lau, Gongyue Tang, Sharon Seow Huang Lim, Xiaowu Zhang
*Institute of Microelectronics, A*STAR, Singapore*
hany@ime.a-star.edu.sg

Technical Session B

Thursday, 6th December
<11:00am - 12:20pm>

Technical Session S-06: Advanced Packaging II

Chair: Dr.Tong Yan Tee — Room: Gemini 2

B-01
ID: 161
11:00am

Critical Factors impacting strength of UBM in smaller and denser bumps and methodologies for optimization

Author(s) - Anandan Ramasamy[1], Inderjit Singh[2], Shin Low[2], Bryant Lin[3]
[1]Xilinx Asia Pacific Ltd, Singapore
[2]Xilinx Inc. San Jose, CA 95124, USA
[3]Xilinx Development Cop. Taiwan Branch
ramasam@xilinx.com

B-06
ID: 245
11:20am

Development of SiC Chip Based Power Package for High Power and High Performance Application

Author(s) - GONG YUE TANG, Leong Ching Wai, Teck Guan Lim, Zhaohui Chen, Yong Liang Ye, Pal Singh Ravinder, Lin Bu, Boon Long Lau, Tai Chong Chai, Kazunori Yamamoto, Xiaowu Zhang
Institute of Microelectronics, Singapore
tangg@ime.a-star.edu.sg

B-11
ID: 196
11:40am

Via Interconnections for Half-Inch Sized Package Fabricated by Minimal Fab

Author(s) - Fumito Imura[1,2], Michihiro Inoue[1], Sommawan Khumpuang[1,2], Shiro Hara[1,2]
[1]National Institute of Advanced Industrial Science and Technology (AIST), Japan
[2]Minimal Fab Promoting Organization
fumito.imura@aist.go.jp

B-16
ID: 274
12:00pm

Evaluation of Materials for Fan-Out Panel Level Packaging (FOPLP) Applications

Author(s) - Nagendra Sekhar Vasarla[1], Srinivasa Rao Vempati[1], Kazunori Yamamoto[1], Fujinaga Tetsushi[2], Jono Koichi[3], Matsui Hiroshi[4], Takaya Yoshiteru[3], Yukio Horiguchi[4]
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[3]SCREEN Finetech Solutions Co., Ltd
[4]SCREEN Semiconductor Solutions
vasarla@ime.a-star.edu.sg

Technical Session S-07: Quality, Reliability & Failure Analysis I

Chair: Mr. Long Haohu — Room: Leo 1

B-02 **ID: 280** 11:00am	**Experimental and Numerical Study on Silicon Die Strength and its Impact on Package Reliability** Author(s) - Jing-en Luan *STMicroelectronics Pte Ltd, Singapore | jing-en.luan@st.com*
B-07 **ID: 211** 11:20am	**Novel concept of an in-situ test system for the thermal-mechanical reliability evaluation of electronic joints** Author(s) - René Metasch[1], Mike Roellig[1], Uwe Naumann[2], Felix Wiesenhuetter[2], Rainer Kaufmann[3] *[1]Fraunhofer Institute for Ceramic Technologies and Systems IKTS, Germany* *[2]Hegewald & Peschke Mess- und Prueftechnik GmbH* *[3]Mytron Bio- und Solartechnik GmbH, Germany* *rene.metasch@ikts.fraunhofer.de*
B-12 **ID: 278** 11:40am	**Evaluation of Fatigue Life of BGA Solder by Unsteady Temperature Cycle** Author(s) - Kento Ogawa *Yokohama National University, Japan | ogawa-kento-hm@ynu.jp*
B-17 **ID: 122** 12:00pm	**Innovative Approach of efficient High Humidity and High Temperature Reverse Bias Testing as significant Qualification Method for Power Electronics Modules**Author(s) - Martin Mueller, Joerg Franke *Friedrich-Alexander University Erlangen-Nuremberg (FAU), Institute for Factory Automation and Production Systems (FAPS), Germany* *martin.mueller@faps.fau.de*

Technical Session S-08: Materials and Processing II

Chair: Zhang, Yanfeng — Room: Leo 2

B-03 **ID: 164** 11:00am	**Solder Resist Crack Resistance Process Characterization in BGA Package for Automotive Grade Reliability** Author(s) - Kesvakumar V C Muniandy[1], Chan Kheng Jin[1], Peter J.L[2] *[1]Infineon Technologies Asia Pacific Pte Lte, Singapore* *[2]Advanced Semiconductor Engineering Group , Kaohsiung, Taiwan* *Kesvakumar.VCMuniandy@infineon.com*
B-08 **ID: 195** 11:20am	**High bonding strength of silver sintered joints on non-precious metal surfaces by pressure sintering under air atmosphere using micro-silver sinter paste** Author(s) - Ly May Chew, Wolfgang Schmitt *Heraeus Deutschland GmbH & Co. KG, Germany* *lymay.chew@heraeus.com*
B-13 **ID: 260** 11:40am	**Electronic Packaging Solution for 300°C Ambience** Author(s) - Vivek Chidambaram[1], Eva Wai Leong Ching[2] *[1]Institute of Microelectronics, A*STAR, Singapore [2]Institute of Microelectronics, A*STAR, Singapore* *nachiappanvc@ime.a-star.edu.sg*
B-18 **ID: 335** 12:00pm	**Mechanical property and plated solder volume effect of Cu core ball** Author(s) - Jae-Yeol Son[1,2], Seul-Gi Lee[1], Yong-Woo Lee[1], Seung-Boo Jung[2] *[1]MKE, Korea, Republic of (South Korea)* *[2]Sungkyunkwan University, Korea, Republic of (South Korea)* *jyson@mke.co.kr*

Technical Session S-09: Electrical Simulation & Characterization I

Chair: Dr. Mihai Rotaru — Room: Leo 3

B-04
ID: 148
11:00am

Dual-attached SMT Capacitor Configurations for Small Form Factor and Single-ended Devices
Author(s) - Chin Lee Kuan[1], Sameer Shekhar[2], Amit K. Jain[2]
[1]Intel Microelectronics, Malaysia
[2]Intel Corporation, Hillsboro, USA
chin.lee.kuan@intel.com

B-05
ID: 190
11:20am

Wideband slot array antenna for 1 THz band imaging device
Author(s) - Kota Tsugami, Tanemasa Asano, Haruichi Kanaya
Kyushu University, Japan
2IE17615E@s.kyushu-u.ac.jp

B-14
ID: 248
11:40am

Inter-Chip Data Transfer Capability of TSV-Free Interposer (TFI) Package
Author(s) - Masaya Kawano, Teck-Guan Lim, Hong-Yu Li
*Institute of Microelectronics, A*STAR, Singapore*
kawanom@ime.a-star.edu.sg

B-19
ID: 282
12:00pm

SIPI Co-Sim: Signal Performance of Super Speed Differential I/O with Power Referencing Design
Author(s) - Li Wern Chew, Paik Wen Ong
Intel Microelectronics (M) Sdn. Bhd., Malaysia
li.wern.chew@intel.com

Technical Session S-10: Mechanical Simulation & Characterization I

Chair: Dr. Kedar Hardikar — Room: Leo 4

B-05
ID: 112
11:00am

Simulation Approach to Predict Warpage based on Resin Curing Behavior during Substrate Manufacturing Process
Author(s) - Masaharu Furuyama, Hideaki Nagaoka, Tomoyuki Akahoshi
FUJITSU LABORATORIES LTD., Japan | mfuruyama@jp.fujitsu.com

B-10
ID: 200
11:20am

Numerical Analysis of the Design and Manufacture of Inkjet Printed Electronics Packaging
Author(s) - Tim Tilford, Stoyan Stoyanov, Chris Bailey
University of Greenwich, United Kingdom | T.Tilford@gre.ac.uk

B-15
ID: 203
11:40am

"3rd Level" Solder Joint Reliability Investigations for Transfer of Consumer Electronics in Automotive Use
Author(s) - Rainer Dudek[1], Marcus Hildebrandt[1], Kerstin Kreyssig[1], Sven Rzepka[1], Ralf Doering[2], Bettina Seiler[2], Thomas Fries[3], Mengjia Zhang[4], Reinhold W. Ortmann[5]
[1]Fraunhofer ENAS, Dept. Micro Materials Center, Chemnitz, Germany
[2]CWM GmbH, Chemnitz, Germany
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Rainer.Dudek@enas.fraunhofer.de

B-20:
ID: 230
12:00pm

Study on Electrical Performance and Mechanical Reliability of Antenna in Package (AIP) with Fan-Out Wafer Level Packaging Technology
Author(s) - Faxing Che, Zihao Chen
IME, Singapore | chef@ime.a-star.edu.sg

Technical Session C

Thursday, 6th December
<02:20pm - 03:40pm>

Technical Session S-11: TSV & WLB Packaging I

Chair: Dr. Minwoo Daniel Rhee — Room: Gemini 2

C-01 **ID: 343** 02:20pm	**High density interconnection for heterogenous intergration on FOWLP platform** Author(s) - Tai Chong Chai, Teck Guan Lim, David Ho, Ser Choong Chong, Faxing Che, Surya Bhattacharya *Institute of Microelectronics, A-STAR, Singapore | chaitac@ime.a-star.edu.sg*
C-06 **ID: 129** 02:40pm	**Combined Thick Resist Processing and Topography Patterning for Advanced Metal Plating** Author(s) - Martin Eibelhuber, Johanna Rimböck, Tobias Zenger, Thomas Uhrmann, Thorsten Matthias *EVGroup, Austria | t.matthias@evgroup.com*
C-11 **ID: 198** 03:00pm	**Design Optimization of Through-Silicon Vias for Substrate-Integrated Waveguides embedded in High-Resistive Silicon Interposer** Author(s) - Matthias Wietstruck[1], Steffen Marschmeyer[1], Selin Tolunay Wipf[1], Christian Wipf[1], Thomas Voß[1], Matthieu Bertrand[3], Emmanuel Pistono[4], Giuseppe Acri[4], Florence Podevin[4], Philippe Ferrari[4], Mehmet Kaynak[1,2] *[1]IHP, Germany [2]Sabanci University, Turkey [3]Laboratoire d'Electronique et Electromagnetisme, Sorbonne Universite, France [4]RFIC-Lab, COMUE University, France* *wietstruck@ihp-microelectronics.com*
C-16 **ID: 240** 03:20pm	**Comprehensive study on die shift and die protrusion issues during molding process of Mold-1st FOWLP** Author(s) - Siak Boon Lim, Ser Choong Chong, Sharon Pei Siang Lim, Wen Wei Seit, Xiaowu Zhang *IME, Singapore | limsb@ime.a-star.edu.sg*

Technical Session S-12: Quality, Reliability & Failure Analysis II

Chair: Prof. Jeff Suhling — Room: Leo 1

C-02 **ID: 363** 02:20pm	**High-resolution 3D X-ray Microscope for Semiconductor Packages Metrology, Quality and Reliability Assessment** Author(s) - John Auyoong, Allen Gu *ZEISS Semiconductor Manufacturing Technology, United States of America* *yowloo.auyoong@zeiss.com*
C-07 **ID: 221** 02:40pm	**Understanding of within Chip variation of optical appearance of Aluminum Pads** Author(s) - Wei Lee Lim[2], Mario Stefenelli[1], Joel Baldevia Agala[3], Evelyn Napetschnig[1] *[1]Infineon Technologies Austria AG, Austria [2]Infineon Technologies (Kulim) Sdn. Bhd, Malaysia [3]Infineon Technologies Batam P.T., Indonesia* *WeiLee.Lim@infineon.com*
C-12 **ID: 142** 03:00pm	**High-resolution Time-domain Reflectometry Analysis in Back-end-of-line (BEOL) by Recursive Circuit Modelling** Author(s) - Yang Shang[1], Makoto Shinohara[2], Rahul Babu Radhamony[3], Joanna Kiljan[3], Alan Wu[3] *[1]Advantest (Singapore) Pte Ltd, Singapore [2]Advantest Corporation, Japan [3]Qualcomm, Inc., USA;* *yang.shang@advantest.com*
C-17 **ID: 111** 03:20pm	**Accelerated Moisture Soak for Moisture Sensitivity Analysis Revisited** Author(s) - Atchareeya Aree-Uea, Amar Mavinkurve, Michiel Van Soestbergen, Rene Rongen, Leo {Jun} Li *NXP Manufacturing (Thailand) Ltd, Thailand* *Leo.l@nxp.com*

Technical Session S-13: Materials and Processing III

Chair: Ms. L.C Tan — Room: Leo 2

C-03
ID: 151
02:20pm

A study of the growth rate of Cu-Sn intermetallic compounds for transient liquid phase bonding during isothermal aging

Author(s) - So-Eun Jeong[1,2], Seung-Boo Jung[2], Jeong-Won Yoon[1]
[1]Korea Institute of Industrial Technology (KITECH), Korea, Republic of (South Korea)
[2]Department of Advanced Materials Engineering, Sungkyunkwan University, Korea, Republic of (South Korea)
soeun@kitech.re.kr

C-08
ID: 171
02:40pm

Dicing Tape Performance in a Plasma Dicing Environment

Author(s) - Stewart Fulton[1], Oliver Ansell[1], Janet Hopkins[1], Richard Barnett[1], Taku Umemoto[2], Takuo Nishida[2]
[1]SPTS Technologies Ltd, United Kingdom [2]LINTEC Advanced Technologies (Europe) GmbH
stewart.fulton@orbotech.com

C-13
ID: 202
03:00pm

Low Transmission Loss Polyimides Substrates: A Novel Alternative to Liquid crystal polymers

Author(s) - Takashi Tasaki
ARAKAWA CHEMICAL INDUSTRIES, LTD., Japan | tasaki@arakawachem.co.jp

C-18
ID: 249
03:20pm

The study of void formation in Ag sinter joint

Author(s) - Ruifen Zhang, Lingling Teo, Dennis Ang
Heraeus material singapore, Singapore | ruifen.zhang@heraeus.com

Technical Session S-14: Emerging Technologies II

Chair: Mr. Christophe Bouquet — Room: Leo 3

C-04
ID: 135
02:20pm

Dynamic Bending Reliability Analysis of Flexible Hybrid Integrated Chip-Foil Packages

Author(s) - Nagarajan Palavesam[1,2], Erwin Yacoub-George[1], Waltraud Hell[1], Christof Landesberger[1], Karlheinz Bock[2], Christoph Kutter[1,3]
[1]Fraunhofer EMFT Research Institution for Microsystems and Solid State Technologies, Munich, Germany [2]Electronics Packaging Laboratory, Technische Universität Dresden, Dresden, Germany [3]Institute of Physics, Universität der Bundeswehr München, Neubiberg, Germany
nagarajan.palavesam@emft.fraunhofer.de

C-09
ID: 349
02:40pm

Stress-Free Aondic Bonding Technology with SW-YY Glass in Comparison to Common Used Borosilicate Glass for Sensitive MEMS

Author(s) - Xiaodong Hu[1,4], Piotr Mackowiak2, Manuel Baeuscher[1,2], Yucheng Zhang[1,2], Bei Wang[3], Ulli Hansen[4], Simon Maus[4], Oliver Gyenge[4], Oswin Ehrmann[1,2], Klaus-Dieter Lang[1,2], Ha-Duong Ngo[1,3]
[1]Technische Universität Berlin, Germany 2Fraunhofer Institute for Reliability and Microintegration, Germany [3]University of Applied Sciences Berlin, Germany [4]MSG Lithoglas GmbH, Berlin, Germany
xiaodonghu2010@googlemail.com

C-14
ID: 192
03:00pm

Guided Interconnect – The Next-Generation Flex Circuits for High-Performance System Design

Author(s) - Jackson Kong, Bok Eng Cheah, Khang Choong Yong, Stephen Hall, Eric Gantner, Chaitanya Sreerama
Intel Corporation | jackson.kong@intel.com

C-19
ID: 275
03:20pm

Integrated Magnetic Inductor Technology on Silicon

Author(s) - Salahuddin Raju[1], Serine Soh[1], Leong Yew Wing[1], David Ho[1], Lin Huamao[1], Marco Stenger Koob[2], Jerzy Wrona[2], Matthias Landmann[2], Berthold Ocker[2], Jürgen Langer[2], Ravinder Pal Singh[1]
*[1]Institute of Microelectronics, A*STAR, Singapore [2]Singulus Technologies, Kahl am Main, Germany*
salahuddin_raju@ime.a-star.edu.sg

Technical Session S-15: Electrical Simulation & Characterization II	
Chair: Dr. Lim Teck Guan	Room: Leo 4
C-05 **ID: 213** 02:20pm	**High Frequency Power Integrity Design Sensitivity to Package Design Rules** Author(s) - Sameer Shekhar[1], Amit Kumar Jain[1], Chin Lee Kuan[2] *[1]Intel Corporation, United States of America [2]Intel Corporation, Malaysia | chin.lee.kuan@intel.com*
C-10 **ID: 302** 02:40pm	**Impedance Characterization of Power Delivery Network in a Flip Chip Package on a Printed Circuit Board** Author(s) - Suat Mooi Low, Fei Guo, Wui Weng Wong *AMD, Singapore | sm.low@amd.com*
C-15 **ID: 110** 03:00pm	**Wafer Level Reliability Characterization of 2.5D IC packages** Author(s) - Jayasanker Jayabalan, Jong Ming Chinq, Vivek Chidambaram Nachiappan, Sharon Lim Pei Siang, Calvin Chua Hung Ming, Surya Bhattacharya *Institute of Microelectronics, Singapore | jayasanker_jayabalan@ime.a-star.edu.sg*
C-20 **ID: 182** 03:20pm	**Accurate Modeling Method of LGA Package for High Power Application** Author(s) - Cheng-Yu Tsai *Advanced Semiconductor Engineering, Inc, Taiwan | Derrick_Tsai@aseglobal.com*

Technical Session D

Thursday, 6th December
<04:40pm - 06:00pm>

Technical Session S-16: Thermal Characterization & Cooling Solutions II	
Chair: Dr. Gamal Refai-Ahmed	Room: Gemini 2
D-01 **ID: 204** 04:40pm	**Stabilizing Flow Boiling Operation of a Microchannel Heat Sink using a Hybrid Geometric Configuration** Author(s) - John Mathew, Poh Seng Lee, Wu Tianqing, Christopher Yap *National University of Singapore | Singapore; e0010771@u.nus.edu*
D-06 **ID: 348** 05:00pm	**Comparison of temperature distributions in modern nanostructures based on different parameters of Dual-Phase-Lag equation** Author(s) - Tomasz Raszkowski, Agnieszka Samson, Mariusz Zubert, Marcin Janicki *Lodz University of Technology Poland | traszk@dmcs.pl*
D-11 **ID: 133** 05:20pm	**Modeling and Control of Hybrid Si-Based Micro-Fluid Cooling System for Data Center Application** Author(s) - Haoran Chen, Yong Han, Gongyue Tang, Xiaowu Zhang *IME A*STAR, Singapore | chen_haoran@ime.a-star.edu.sg*
D-16 **ID:136** 05:40pm	**RSSDs Thickness Impact on Storage System and Assessment by Pseudo Curve** Author(s) - Feng Qi, Casey Winkle, Xudong Tang *Intel | feng.a.qi@intel.com*

Technical Session S-17: Interconnect Technologies II

Chair: Mr. Eric Perfecto — Room: Leo 1

D-02 **ID: 283** 04:40pm	**An Evaluation of the Electrical Stability of Copper Filled Isotropic Conductive Adhesives in High Moisture Environments** Author(s) - Shanda Wang, David Hutt, David Whalley, Gary Critchlow *Loughborough University, United Kingdom | D.A.Hutt@lboro.ac.uk*
D-07 **ID: 187** 05:00pm	**Research on the effect of bonding properties of micro bumps for different morphology and interconnection methods** Author(s) - Fengwei Dai[1,2,3], David Wei Zhang[1], Meiying Su[2,3], Guojun Wang[3], Dengfeng Yang[3], Wenqi Zhang[2,3], Liqiang Cao[2,3] *[1]School of Microelectronics, Fudan University* *[2]Institute of microelectronics of Chinese academy of sciences* *[3]The National Center for Advanced Packaging, China, People's Republic of* *fengweidai@ncap-cn.com*
D-12 **ID: 332** 05:20pm	**Cracking failure of Cu pillar bump caused by electromigration and stress concentration under thermo-electric coupling loads** Author(s) - Si Chen, Bin Zhou, Zhizhe Wang, Yunfei En, Yun Huang, Bin Yao *China electronic product reliability and environmental testing research institute, China, People's Republic of | chensiceprei@yeah.net*
D-17 **ID: 355** 05:40pm	**Fine Pitch Cu to Cu interconnects for 2.5D Packaging** Author(s) - Ling Xie, Ser Choong Chong, Vasarla Nagendra Sekhar, Daniel Ismael Cereno, Sunil Wickramanayaka *Institute of Microelectronics, A*STAR, Singapore | xieling@ime.a-star.edu.sg*

Technical Session S-18: Materials and Processing IV

Chair: Mr.Alvin Lee — Room: Leo 2

D-03 **ID: 225** 04:40pm	**Laser Separation of Dissimilar Substrates Using Water Washable Materials** Author(s) - John Cleaon Moore[1], Stefan Quandt[2] *[1]Daetec LLC, United States of America* *[2]Trumpf, Inc., United States of America* *jmoore@daetec.com*
D-08 **ID: 257** 05:00pm	**Enhancing Productivity for IC-substrate manufacturing by using a novel Copper Electrolyte for Semi Additive Plating** Author(s) - Mustafa Özkök[1], Olivier Mann[1], Toshiya fujiwara[2] *[1]Atotech Deutschland GmbH, Germany* *[2]Atotech Japan K.K.* *mustafa.oezkoek@atotech.com*
D-13 **ID: 288** 05:20pm	**Isoconversional Method for the Modeling of the Curing Kinetics of Epoxy Molding Compounds for Mold Process Simulation** Author(s) - Tamas Deak[1], David O. Kazmer[2] *[1]Philips Lighting Hungary Kft., Hungary* *[2]University of Massachusetts Lowell* *tamas.deak@signify.com*
D-18 **ID: 354** 05:40pm	**Modeling and simulation of chemical amplification photoresist to produce high-density cone-shaped micro bumps** Author(s) - Daiki Kumagawa, Mamoru Sakamoto, Yohei Aoki, Tanemasa Asano *Kyushu University, Japan* *asano@ed.kyushu-u.ac.jp*

Technical Session S-19: Emerging Technologies III

Chair: Dr. Gokul Kumar — Room: Leo 3

D-04 **ID: 237** 04:40pm	**Magnetic Shielding and Packaging of STT MRAM** Author(s) - Teck Guan Lim[1], Boo Yang Jung[2], Leong Ching Wai[1] *[1]Institute of Microelectronics, Singapore [2]GLOBALFOUNDRIES Singapore Pte Ltd* *limtg@ime.a-star.edu.sg*
D-09 **ID: 170** 05:00pm	**Implementation of High-Temperature Pressure Sensor Package and Characterization up to 500 °C** Author(s) - Nilavazhagan Subbiah[1], Qingming Feng[1], Kevin Ali Beltran Ramirez[1], Jürgen Wilde[1], Gudrun Bruckner[2] *[1]IMTEK, University of Freiburg, Germany [2]CTR AG, HIT Villach, Austria* *subbiah@imtek.de*
D-14 **ID: 128** 05:20pm	**Multilayer Roll-to-Roll Screen-Printing for Printed Electronics Applications** Author(s) - Budiman Salam, X.C Shan, Zhanhong Cen, B.K. Lok *Singapore Institute of Manufacturing Technology, Singapore | budimans@simtech.a-star.edu.sg*
D-19 **ID: 163** 05:40pm	**Fabrication and Packaging of surface electrode ion trap for quantum computing** Author(s) - Jing Tao, Nam Piau Chew, Chuan Seng Tan *Nanyang Technological University, Singapore | taojing@ntu.edu.sg*

Technical Session S-20: Mechanical Simulation & Characterization II

Chair: Dr. Rainer Dudek — Room: Leo 4

D-05 **ID: 207** 04:40pm	**Processing Models Based on Stress Conservation Law Utilized for Temperature-Dependent Warpage Prediction of MUF FCCSP with 3L ETS** Author(s) - Chih-Sung Chen, Nicholas Kao, Poyu Liao, Ssu-Cheng Lai, Don Son Jiang *Siliconware Precision Industries Co. Ltd., Taiwan | chihsungchen@spil.com.tw*
D-10 **ID: 298** 05:00pm	**Design of Micro-sensors for Measuring Localised Stresses during Fan-Out Wafer Level Packaging (FOWLP) Processes** Author(s) - Xiaowu Zhang, Zhaohui Chen, Boon Long Lau, Yong Han, Sharon Pei Shang Lim, Simon Siak Boon Lim *IInstitute of Microelectronics, Singapore | xiaowu@ime.a-star.edu.sg*
D-15 **ID: 181** 05:20pm	**Numerical analysis of laser thermal compression bonding for flip chip package** Author(s) - Youngmoon Jang[1], Byoung-Ho Ko[1], Hoon Sun Jung[2], Jin Wook Jeong[3], Sung-Hoon Choa[2] *[1]Dept. Of Manufacturing System and Design Engineering Seoul National University of Science and Technology, Seoul [2]Graduate School of Nano IT Design Fusion, Seoul National University of Science and Technology, Seoul, 01811, Republic of Korea [3]R&D Center New Product Development team, HANA Micron Inc, Seongnam-Si, Korea* *youngmoon1010@gmail.com*
D-20 **ID: 334** 05:40pm	**Warpage prediction and stress analysis for large size through-silicon-via interposer package** Author(s) - Meiying Su[1,2], Jun Li[1,2], Liqiang Cao[1,2] *[1]Institute of Microelectronics of the Chinses Academy of Sciences, China, People's Republic of [2]National Center for Advanced Packaging Co., Ltd* *sumeiying@ime.ac.cn*

Technical Session E

Friday, 7th December
<09:00am - 10:20am>

Technical Session S-21: TSV & WLB Packaging II

Chair: Dr. Han-Ping Pu — Room: Gemini 2

E-01 **ID: 319** 09:00am	**Development of cost effective Copper overburden removal for Via-Last TSV fabrication** Author(s) - Qin Ren, Woon Leng Loh, Xiang Yu Wang *Institue of Microelectronics, A*star, Singapore	renq@ime.a-star.edu.sg*
E-06 **ID: 153** 09:20am	**One Micron Damascene Redistribution for Fan-Out Wafer Level Packaging using a Photosensitive Dielectric Material** Author(s) - Robert Hsieh[1], Warren W Flack[1], Ha-Ai Nguyen[1], John Slabbekoorn[2], Samuel Suhard[2], Andy Miller[2], Akito Hiro[3], Romain Ridremont[3] *[1]Ultratech, a division of Veeco [2]IMEC [3]JSR MICRO NV* *rhsieh@ultratech.com*
E-11 **ID: 208** 09:40am	**The Robust WLCSPs : enabling 5-side protection** Author(s) - Seung YOON[1], Tony Chen[2] *[1]Statschippac PTE LTD, JCET Group, Singapore [2]JCAP, JCET Gorup, China* *Seungwook.yoon@statschippac.com*
E-16 **ID: 239** 10:00am	**Process Development of Fan-Out interposer with Multi-layer RDL for 2.5D System in Package** Author(s) - Hsiang-Yao Hsiao, Soon Wee Ho, Siak Boon Lim, Ser Choong Chong, Pei Siang Lim, Tai Chong Chai *Astar-IME, Singapore	hsiaohy@ime.a-star.edu.sg*

Technical Session S-22: Interconnect Technologies III

Chair: Mr.Sam Karikalan — Room: Leo 1

E-02 **ID: 149** 09:00am	**Develop Smart Wire Bonding Processes for Smart Factories** Author(s) - Ivy Qin, Aashish Shah, Basil Milton, Gary Schulze, Nelson Wong, Andrew Chang *kulicke and soffa ind. inc, United States of America	ckchang@kns.com*
E-07 **ID: 123** 09:20am	**Investigations of Silver Sintered Interconnections on 3-Dimensional Ceramics with Plasma Based Additive Copper Metallizations** Author(s) - Alexander Hensel[1], Christian Schwarzer[2], Matthias Scheetz[1], Michael Kaloudis[2], Joerg Franke[1] *[1]Friedrich-Alexander University Erlangen-Nürnberg, Germany;* *[2]Aschaffenburg University of Applied Science* *alexander.hensel@faps.fau.de*
E-12 **ID: 174** 09:40am	**Low-temperature Cu-Cu bonding by self-reduction of particle-free Ag ion paste** Author(s) - Junjie Li, Tielin Shi, Guanglan Liao, Zirong Tang *Huazhong University of Science and Technology, China, People's Republic of	junjieli@hust.edu.cn*
E-17 **ID: 338** 10:00am	**New Alternative Metal Coated Silver bonding wire for Gas-Free bonding and High Reliability Performance** Author(s) - SangYeob Kim, SungMin Jeon, ChongMin Park, ByungHoon Jung, SeungHyoun Kim, JeongTak Moon *MK Electron Co., Ltd, Korea, Republic of (South Korea)	kimsy@mke.co.kr*

Technical Session S-23: Materials and Processing V

Chair: Dr.Dongshun Bai — Room: Leo 2

E-03 **ID: 172** 09:00am	**In-situ Cure Shrinkage Characterization of Epoxy Molding Compounds for FOWLP** Author(s) - Xiaobai Wang[1], Yosephine Andriani[1], Songlin Liu[1], Zhaohui Chen[2], Xiaowu Zhang[2] *[1]Institute of Materials Research and Engineering, A* Star, Singapore* *[2]Institute of Microelectronics, A* star, Singapore* *wangxb@imre.a-star.edu.sg*
E-08 **ID: 217** 09:20am	**Resolving Plating, stripping, etching challenges for shrinking dimension in advanced packaging** Author(s) - Kok Guan Ng, Jerome Daviot *TECHNIC ASIA PACIFIC PTE LTD, Singapore | jerome.daviot@technic.fr*
E-13 **ID: 361** 09:40am	**Preparation and mechanical characterization of Ni-Fe-P coating for power electronics** Author(s) - Li Liu[2], Juan Peng[2], Sheng Liu[1], Zhiwen Chen[1] *[1]Wuhan University, China, People's Republic of* *[2]Wuhan University of Technology, China, People's Republic of* *zhiwen.chen@whu.edu.cn*
E-18 **ID: 266** 10:00am	**Effect of the Strengthening Mechanism on the Response of a Solder Alloy to Strain Rate and Ageing** Author(s) - Wayne Chee Weng Ng[1], Tetsuya Akaiwa[1], Pavithiran Narayanan[2], Keith Sweatman[1], Tetsuro Nishimura[1], Takatoshi Nishimura[1] *[1]Nihon Superior Co., Ltd., Japan [2]Nihon Suuperior (M) Sdn. Bhd.* *wayne@nihonsuperior.co.jp*

Technical Session S-24: Emerging Technologies IV

Chair: Dr.Tanja Braun — Room: Leo 3

E-04 **ID: 329** 09:00am	**Development of Three Dimensional Roll-up Polymer-Si Structure for Nerve Ablation Catheter** Author(s) - Ruiqi Lim, Weiguo Chen, David Sze Wai Choong, Maria Ramona Damalerio, Ming-Yuan Cheng *Institute of Microelectronics, Singapore | chenwg@ime.a-star.edu.sg*
E-09 **ID: 289** 09:20am	**Integration of Tungsten micro-heaters and polymer microfluidic for the cell sorting application.** Author(s) - Bivragh Majeed, Lut Van Acker, Koen De Wijs, Chengxun Liu *imec, Belgium | bivragh.majeed@imec.be*
E-14 **ID: 331** 09:40am	**Development of a Flexible Printed Multi-Functional Sensor Platform for Medical Applications** Author(s) - David Choong, Ruiqi Lim, Maria Ramona, Weiguo Chen, Ming Yuan Cheng *ASTAR Institute of Microelectronics, Singapore | david_choong@ime.a-star.edu.sg*
E-19 **ID: 328** 10:00am	**Molecular Dynamics Simulation of GaN Nano-grinding** Author(s) - Yixin Xu[1], Fulong Zhu[1], Miaocao Wang[1], Xiaojian Liu[1], Sheng Liu[2] *[1]Huzahong University of Science and Technology, People's Republic of China* *[2]Wuhan University, People's Republic of China* *xuyixin@hust.edu.cn*

Technical Session S-25: Thermal Characterization & Cooling Solutions III	
Chair: Prof. Robert Kao	Room: Leo 4
E-05 **ID: 159** 09:00am	**Spray cooling enhancement studies using dielectric liquid** Author(s) - Feng Qi, Casey Winkle, Xudong Tang *Ranjith Kandasamy, Pengfei Liu, Huicheng Feng, Teck Neng Wong, Kok Chuan TohTechnological University, Singapore | ranjith.k@ntu.edu.sg*
E-10 **ID: 209** 09:20am	**Experimental Study of Ageing Effect in Pool Boiling Heat Transfer** Author(s) - Tianqing Wu, Poh Seng Lee, John Mathew, Si Rong Lu *National University of Singapore, Singapore | e0010746@u.nus.edu*
E-15 **ID: 228** 09:40am	**Design, Fabrication and Characterization of a Compact Mini Heat Exchanger for Data Centre Cooling Applications** Author(S) - Gong Yue Tang, Yong Han, Haoran Chen, Xiaowu Zhang *Institute of Microelectronics, Singapore | tangg@ime.a-star.edu.sg*
E-20 **ID: 254** 10:00am	**A Low Computational Cost and Accurate Thermal Calculation Method for Multi-hotspot IC** Author(s) - Daixing Wang[1], Yudan Pi[1,2], Wei Wang[2,3], Yufeng Jin[1,2,3] *[1]School of Electronic and Computer Engineering, Peking University Shenzhen Graduate School, Shenzhen, Guangdong, China* *2Institute of Microelectronics, Peking University, Beijing, China* *[3]National Key Lab of Micro/Nano Fabrication Technology, Peking University, Beijing, China* *dxwang1215@pku.edu.cn*

Technical Session F

Friday, 7th December
<11:10am - 12:30pm>

Technical Session S-26: Advanced Packaging III	
Chair: Mr. Chai Tai Chong	Room: Gemini 2
F-01 **ID: 165** 11:10am	**Active Device Performance after Fan-out Wafer-level Packaging Process** Author(s) - Hongyu Li, Masaya Kawano, Simon Lim, Daniel Ismael Cereno, Vasarla Nagendra Sekhar *IME, Singapore | lihy@ime.a-star.edu.sg*
F-06 **ID: 139** 11:30am	**Temporary Bonding Material Study for Room Temperature Mechanical Debonding with eWLB Wafer Application** Author(s) - Seiya Masuda[1], Yu Iwai[1], Mitsuru Sawano[1], Kotaro Okabe[1], Kazuto Shimada[1], Joal Caparas[2], Won Kyoung Choi[2] *[1]FUJIFILM Corporation, Japan* *[2]STATS ChipPAC Ltd, Singapore* *seiya.masuda@fujifilm.com*
F-11 **ID: 347** 11:50am	**Development of Antenna in FO-WLP** Author(s) - Serine Soh, David Ho, Hsiang Yao Hsiao, Simon Lim, Sharon Lim, Ser Choong Chong, Tai Chong Chai *Institute of Microelectronics, Singapore* *sohsb@ime.a-star.edu.sg*
F-16 **ID: 154** 12:10pm	**Study of the die potion accuracy in the fabrication process of a die first type FO-PLP** Author(s) - Keisuke Nishido, Hitoshi Onozeki, Naoya Suzuki, Toshihisa Nonaka *Hitachi Chemical Co.,Ltd., Japan* *k-nishido@hitachi-chem.co.jp*

Technical Session S-27: Equipment and Process Automation

Chair: Mr.Lee, Chee Ping — Room: Leo 1

F-02 **ID: 262** 11:10am	**Enhancing Bump Thick Resist Lithography: Establishing Process Controls to Eliminate Copper Pillar Footing** Author(s) - Jose Arvin Matute Plomantes, Ruby Ann Dizon Mamangun, Armando Tresvalles Clarina Jr., Jamel Penuliar Cayabyab, Rafael Jose L. Guevara *Texas Instruments Phils, Philippines	j-plomantes@ti.com*
F-07 **ID: 188** 11:30am	**Millimeter Wave Antenna in Package (AiP) Measured in Far-Field by a Vertical Probe Station** Author(s) - Bo-Siang Fang[1], Kuan-Ta Chen[1], Cha-Chu Lai[1], Jui-Ching Cheng[2] *[1]Siliconware Precision Industries Co., Ltd., Taiwan* *[2]National Taipei University of Technology* *boxiangfang@spil.com.tw*
F-12 **ID: 357** 11:50am	**Critical Surface Quality inspection and analysis of precision optical components fabricated using CMP methods** Author(s) - Venkata Ramana Pamidighantam[1], Mahender Kumar Gupta[2], Krishna Rao Guntuku[2] *[1]Vasavi College Of Engineering, Hyderabad India* *[2]Electro Optical Instruments Research Academy, Hyderabad, India* *pvramana@staff.vce.ac.in*
F-17 **ID: 364** 12:10pm	**Wafer Level Through-polymer Optical Vias (TPOV) Enabling High Throughput of Optical Windows Manufacturing** Author(s) - Johan Hamelink *Boschman Technologies, Netherlands	johanhamelink@boschman.nl*

Technical Session S-28: Materials and Processing VI

Chair: Mr. Santosh Kumar — Room: Leo 2

F-03 **ID: 238** 11:10am	**Process Development of micro-bump flip chip bonding with Non-Conductive Film** Author(s) - Ser Choong Chong, Hongyu Xie, Ling Xie, Daniel Ismael Cereno *Institute of Microelectronics, Singapore	chongsc@ime.a-star.edu.sg*
F-08 **ID: 255** 11:30am	**Phthalonitrile (PN) based electronic packages for High Temperature Applications** Author(s) - Eric Jian Rong Phua[1,2], Ming Liu[3], Jacob Song Kiat Lim[1,3], Bokun Cho[4], Chee Lip Gan[1,3] *[1]School of Materials Science and Engineering [2]School of Chemical and Biomedical Engineering* *[3]Temasek Laboratories@NTU [4]Energetics Research Institute* *jrphua@ntu.edu.sg*
F-13 **ID: 244** 11:50am	**Material Selection for Ion Trap Chip Working at Extreme Low Temperatures** Author(s) - Lin Bu *IME, Singapore	bul@ime.a-star.edu.sg*
F-18 **ID: 311** 12:10pm	**Gold Passivated Cu-Cu Bonding At 140˚C For 3D IC Packaging And Heterogeneous Integration Applications.** Author(s) - Satish Bonam, Hemanth Kumar Cheemalamarri, Siva Rama Krishna Vanjari, Shiv Govind Singh *Indian Institute of Technology Hyderabad, India	ee16resch01006@iith.ac.in*

Technical Session S-29: Electrical Simulation & Characterization III

Chair: Dr. Stevan Hunter — Room: Leo 3

F-04
ID: 253
11:10am

K-band SATCOM Receiver Modules: System Design, Analysis and Test using the M3-Approach
Author(s) - Christian Tschoban, Ivan Ndip
Fraunhofer IZM, Germany | christian.tschoban@izm.fraunhofer.de

F-09
ID: 304
11:30am

Crystal Oscillator Interconnect Architecture with Noise Immunity
Author(s) - Raymond Chong, Khang Choong Yong
Intel Microelectronics Sdn Bhd, Malaysia | raymond.chong@intel.com

F-14
ID: 306
11:50am

Cost Effective Capacitive Testing for RDL First
Author(s) - Keita Gunji, Toshihisa Hibarino
Nidec Read Corporation, Japan | k.gunji@nidec-read.co.jp

F-19
ID: 134
12:10pm

Simulation And Electrical Characterization Of A Novel 2D-Printed Incontinence Sensor With Conductive Polymer PEDOT:PSS For Medical Applications
Author(s) - Manuel Baeuscher[1,2], Xiaodong Hu[2], Piotr Mackowiak[1], Oswin Ehrmann[1], Klaus-Dieter Lang[1,2], Ha-Duong Ngo[1,3]
[1]Fraunhofer Institute for Reliability and Microintegration Berlin
[2]Technical University Berlin [3]University of Applied Sciences Berlin
Manuel.Baeuscher@izm.fraunhofer.de

Technical Session S-30: Mechanical Simulation & Characterization III

Chair: Dr.Zhang Xiaowu — Room: Leo 4

F-05
ID: 234
11:10am

Solder Joint Reliability Simulation of Fan-out Wafer Level Package Considering Visco-Elastic Material Properties
Author(s) - Zhaohui Chen
IME A-Star, Singapore, Singapore | chenz@ime.a-star.edu.sg

F-10
ID: 232
11:30am

Mechanical Characterization of MEMS-Microphones by means of Nanoindentation and Coupled Finite Element Analysis
Author(s) - Jan Albrecht[1], Marie Weissbach[1], Matthias Vobl[2], Ulrich Krumbein[2], Sven Rzepka[1]
[1]Fraunhofer Institute for Electronic Nano Systems ENAS,
Technologie-Campus 3, 09126 Chemnitz, Germany
[2]Infineon Technologies, Am Campeon 1-15, 85579 Neubiberg, Germany
jan.albrecht@enas.fraunhofer.de

F-15
ID: 173
11:50am

Dynamic Mechanical Analysis and Viscoelastic Behavior of Epoxy Molding Compounds for FOWLP
Author(s) - Xiaobai Wang[1], Yosephine Andriani[1], Songlin Liu[1], Zhaohui Chen[2], Xiaowu Zhang[2]
[1]Institute of Materials Research and Engineering, A Star, Singapore*
[2]Institute of Microelectronics, A star, Singapore*
wangxb@imre.a-star.edu.sg

F-20
ID: 199
12:10pm

Constitutive Behaviour of Single Lap Joint of Sintered Silver Paste
Author(s) - Xu Long[1], Chongyang Du[1], Wenbin Tang[1], Yongchao Liu[2], Yao Yao[1], Fengrui Jia[3]
[1]School of Mechanics, Civil Engineering and Architecture,
Northwestern Polytechnical University, Xi'an, China
[2]College of Mining Engineering, Liaoning Shihua University, Fushun, China
[3]College of Petroleum Engineering, Liaoning Shihua University, Fushun, China
xulong@nwpu.edu.cn

Technical Session G

Friday, 7th December
<02:00pm - 03:20pm>

Technical Session S-31: TSV & WLB Packaging III		
Chair: Dr. Seung Wook Yoon		Room: Gemini 2
G-01 **ID: 316** 2:00pm	**EPIC Via Last on SOI wafer integration challenges** Author(s) - Woon Leng Loh *Institute Of Microelectronics, Singapore | woonlloh@yahoo.com.sg*	
G-06 **ID: 210** 2:20pm	**Within Die Coplanarity Improvement Strategies for Electroplated Cu Pillars** Author(s) - Gabe Graham, Lee Peng Chua, Bryan Buckalew, Thomas Ponnuswamy, Steve Mayer *Lam Research, United States of America | gabe.graham@lamresearch.com*	
G-11 **ID: 222** 2:40pm	**Hybrid Cu-SiN and Cu-SiOx Direct Bonding of 200 MM CMOS Wafers With Five Metal Levels: Morphological, Electrical and Reliability Characterization** Author(s) - Celso Cavaco, Konstantinos Chatzinis, Bert van Lijnschoten, Stefano Guerrieri *Imec, Belgium | cavaco@imec.be*	
G-16 **ID: 346** 3:00pm	**Development of FO-WLP Package-on-Package using RDL-first Integration Flow** Author(s) - Soon Wee Ho, Hsiang-Yao Hsiao, Siak Boon Lim, Leong Ching Wai, Ser Choong Chong, Pei Siang Lim, Tai Chong Chai *Institute of Microelectronics, Singapore | hosw@ime.a-star.edu.sg*	

Technical Session S-32: Interconnect Technologies IV		
Chair: Prof. Gan Chee Lip		Room: Leo 1
G-02 **ID: 243** 2:00pm	**Challenges and Approaches of 2.5D high density Flip chip interconnect on through mold interposer** Author(s) - Sharon Pei Siang Lim, Ser Choong Chong, Wenwei Seit, Tai Chong Chai *IME, Singapore | limps@ime.a-star.edu.sg*	
G-07 **ID: 184** 2:20pm	**High Density metal alloy Interconnections Using Novel Wafer Bonding Approach For 3D IC Packaging Applications** Author(s) - Hemanth Kumar Cheemalamarri, Satish Bonam, Siva Rama Krishna Vanjari, Shiv Govind Singh *Indian Institute of Technology Hyderabad, India | ee16resch01006@iith.ac.in*	
G-12 **ID: 263** 2:40pm	**Enabling Flip Chip QFN Technology: Understanding Kirkendall Voiding and Factors Affecting its Formation during Bumping Process** Author(s) - Ruby Ann Dizon Mamangun, Rafael Jose Lizares Guevara, Jose Arvin Matute Plomantes *Texas Instruments Philippines, Inc., Philippines | r-mamangun@ti.com*	
G-17 **ID: 156** 3:00pm	**Analysis of Low Profile Ferrite Material Based Planar Shell Core Inductor** Author(s) - Zeeshan Umar[1], Maciej Wojnowsk[1], Franz Xaver Engelsberger[1], Amelie Hagelaue[2], Robert Weigel[2] *[1]Infineon Technologies, Germany [2]University Erlangen-Nuremberg* *zeeshan.umar@infineon.com*	

Technical Session S-33: Quality, Reliability & Failure Analysis III

Chair: Mr. Keith Newman — Room: Leo 2

G-03 **ID: 314** 2:00pm	**Electrostatically induced voltages generated in ungrounded metal box and on the box when charged body moves away from the box** Author(s) - Norimitsu Ichikawa *Kogakuin University, Japan | ichikawa@cc.kogakuin.ac.jp*
G-08 **ID: 169** 2:20pm	**Evaluation of Thermal Crack Propagation in Die-attached Joints Due to Cyclic Energization by Synchrotron Radiation Laminography Monitoring** Author(s) - Junya Ooi[1], Toshihiko Sayama[2], Hiroyuki Tsuritani[2], Yoshiyuki Okamoto[3], Masato Hoshino[4], Kentaro Uesugi[4], Takao Mori[1] *[1]Department of Mechanical System Engineering, Toyama Prefectural University, Japan [2]Machinery & Electronics Research Institute, Toyama Industrial Technology Development Center, Japan [3]Design Engineering Department, Cosel Co., Ltd., Japan [4]SPring-8, Japan Synchrotron Radiation Research Institute (JASRI) t753002@st.pu-toyama.ac.jp*
G-13 **ID: 267** 2:40pm	**Effect of the laser parameters, epoxy mold compound properties and mold tool surface finishing on mark legibility of encapsulated IC package** Author(s) - Ming Siong Lim, Yuan Tat Chai *Infineon Technologies, Malaysia | MingSiong.Lim@infineon.com*
G-18 **ID: 315** 3:00pm	**An Alternative Packaging Solution in Achieving Moisture Sensitivity Level One (1) for Small Outline Integrated Circuit (SOIC) Automotive Packages** Author(s) - Alvin Denoyo, Rod Delos Santos Jr., Darwin De Lazo, Ivan Gil Costa, Allen Menor *ON Semiconductor, Philippines | Alvin.Denoyo@onsemi.com*

Technical Session S-34: Emerging Technologies V

Chair: Dr.Kripesh Vaidyanathan — Room: Leo 3

G-04 **ID: 193** 2:00pm	**Dual-band differential outputs CMOS Low Noise Amplifier** Author(s) - Atsuhiro Hamasawa, Haruichi Kanaya *KyushuUniversity/Japan, Japan | 2IE17603Y@s.kyushu-u.ac.jp*
G-09 **ID: 330** 2:20pm	**Development of Deployable Catheter for Minimally Invasive Surgery Guidewire Application** Author(s) - Weiguo Chen, Ramona Ramona, Ruiqi Lim, David Choong, Ming-Yuan Cheng *Institute of Microelectronics (IME), Singapore | chenwg@ime.a-star.edu.sg*
G-14 **ID: 150** 2:40pm	**Design and optimization of the 10Tbps optical transmission system** Author(s) - Huimin He[1,2], Fengman Liu[1,2], Haiyun Xue[1,2], Yu Sun[1,2], Liqiang Cao[1,2] *[1]Institute of Microelectronics of Chinese Academy of Sciences [2]National Center for Advanced Packaging Co.LTD hehuimin@ime.ac.cn*
G-19 **ID: 303** 3:00pm	**High Performance Package-Level EMI shielding of Ag Epoxy Composites with Spray method for High Frequency FCBGA package Application** Author(s) - Kisu Joo, Kyu Jae Lee, Jung Woo Hwang, Jin-Ho Yoon, Yoon-Hyun Kim, Se Young Jeong *Ntrium Inc., Korea, Republic of (South Korea) | ksjoo@ntrium.com*

Technical Session S-35: Thermal Simulation and Modeling IV	
Chair: Prof Tan Chun Seng	Room: Leo 4
G-05 **ID: 295** 2:00pm	**Extending cooling limit of RRU based on level 1 thermal management** Author(s) - Gamal Refai-Ahmed, Hoa Do, Brian Philofsky, Anthony Torza *Xilinx Inc., United States of America | hoa.do@xilinx.com*
G-10 **ID: 333** 2:20pm	**A novel double-layered heat sink for high power electronics** Author(s) - Yicang Huang[1], Hui Li[1], Shengnan Shen[1], Shiyue Ma[2] *[1]Wuhan University, China, People's Republic of China* *[2]Tongji University, China, People's Republic of China* *huang_yicang@whu.edu.cn*
G-15 **ID: 242** 2:40pm	**Mold Flow Simulation for Fan-out Panel-Level Packaging (FOPLP)** Author(s) - Lin Bu *IME, Singapore | bul@ime.a-star.edu.sg*
G-20 **ID: 336** 3:00pm	**Electromigration Modeling for 3D-IC TSV Interconnect considering grain structure** Author(s) - Yuanxiang Zhang, Sijia Yu, Deqi Su, Zhipeng Shen *Quzhou University, China, People's Republic of | zhangyx@qzu.zj.cn*

Interactive Session 1

Thursday, 6th December
Room: Pisces
<10:00am - 11:00am> - <3:40pm - 4:40pm)

ID: 104	**Kirkendall Voids Improvement in Thin Small No Lead Package** Author(s) - Lay Yeap Lim, Yau Huang Huang *Infineon Technologies Sdn Bhd, Malaysia | layyeap.lim@infineon.com*
ID: 105	**Characterization of interfacial intermetallic compounds in gold wire bonding with copper pad** Author(s) - Bisheng Wang[1], Lois JinZhi Liao[2], Xiaomin Li[2], Younan Hua[2], Chao Fu[2] *[1]Huawei Technologies Co Ltd [2]WinTech Nano-Technology Services Pte. Ltd* *lois@wintech-nano.com*
ID: 114	**Failure Analysis on Mobile Phone Batteries and Accessories** Author(s) - ZHI JIN[1], HIroshi NISHIKAWA[1], Y.C Chan[2] *[1]Osaka Univerisity, Japan [2]City University of Hong Kong, China* *jinzhi711@gmail.com*
ID: 117	**High modulus DAF Introduction to decrease thin die WB crack issue** Author(s) - Ling Yang, Allen Ji *Sandisk/Western Digital, China, People's Republic of | Linda.yang@wdc.com*
ID: 120	**Effect of electric current on constitutive behaviour and microstructure of SAC305 solder joint** Author(s) - Wenbin Tang[1], Xu Long[1], Yongchao Liu[2], Chongyang Du[1], Yao Yao[1], Cheng Zhou[3], Peiyan Wu[3], Fengrui Jia[4] *[1]School of Mechanics, Civil Engineering and Architecture, Northwestern Polytechnical University, Xi'an, China [2]College of Mining Engineering, Liaoning Shihua University, Fushun, China [3]Space Research Institute of Electronics and Information Technology, Aerospace Science and Technology Corporation, Xi'an, China [4]College of Petroleum Engineering, Liaoning Shihua University, Fushun, China* *xulong@nwpu.edu.cn*
ID: 125	**Void Defect Formed in Wiping Step of Gravure Printing** Author(s) - Zhanhong Cen, Xuechuan Shan, Budiman Salam, Lee Siew Rachel Tan, Jun Wei *Singapore Institute of Manufacturing Technology, Singapore* *cen_zhanhong@simtech.a-star.edu.sg*
ID: 130	**Research on Feedforward Control in the linear motor direct drive XY two-dimensional platform** Author(s) - Yunbo He, Zuoxiong He *Key Laboratory of Precision Microelectronic Manufacturing Technology & Equipment of Ministry of Education, School of Electromechanical Engineering, Guangdong University of Technology, Guangzhou, P.R.China* *hezx0214@outlook.com*
ID: 132	**Development of Thermal Test Package for Data Center Micro-Fluid Cooling Characterization** Author(s) - Yong Han, Boon Long Lau, Gongyue Tang, Sharon Seow Huang Lim, Xiaowu Zhang *Institute of Microelectronics, A*STAR, Singapore | hany@ime.a-star.edu.sg*

ID: 138	**How my electronics is influenced by housing: A Thermal Point of View Study to Understand the Impact of Housing on Internal Air Temperature** Author(s) - Nitesh Kumar Sardana, Kratika Shrivastava *Robert Bosch Engineering and Business Solution Pvt Ltd, India* *niteshkumar.sardana@in.bosch.com*
ID: 143	**Study of polysilsesquioxane dielectric for the use of multi-structured redistribution layers in fan-out wafer level packaging applications** Author(s) - Changmin Song, Sungdong Kim, Sarah Eunkyung Kim* *Seoul National University of Science and Technology, Korea, Republic of (South Korea)* *211x924@naver.com*
ID: 144	**High Aspect Ratio~10 TSV Via-last-from-back Process Development and Integration** Author(s) - Xiangyu wang, Hongyu Li *wangxy@ime.a-star.edu.sg*
ID: 146	**Joint Feature Automatic Classification for Aluminum Wire Bonding Based on KPCA and Random Forest** Author(s) - zhili long, xing zhou, xiaobing zhang, ronghua he *Harbin Institute of Technology Shenzhen Graduate School, China, People's Republic of* *longzhili@hit.edu.cn*
ID: 147	**Effect of Ar-N2 Plasma Treatment on Copper Surface for Cu-Cu Wafer Bonding** Author(s) - Hae-Sung Park, Sarah Eunkyung Kim* *Seoul National University of Science and Technology, Korea, Republic of (South Korea)* *haesung89@seoultech.ac.kr*
ID: 152	**Numerical Investigation on the Condensation Heat Transfer of FC72 in the Presence of Air** Author(s) - Pengfei Liu, Huicheng Feng, Kandasamy Ranjith, Teck Neng Wong, Kok Chuan Toh *Nanyang Technological University, Singapore | pengfei001@e.ntu.edu.sg*
ID: 155	**Study on bottom-up Cu filling process for Through Silicon Via (TSV) metallization** Author(s) - Gilho Hwang, Hsiang-Yao Hsiao, David Soon Wee Ho *Institute of Microelectronics, Singapore | hwangg@ime.a-star.edu.sg*
ID: 158	**Coated Silver Wire Bond: Reliability of Epoxy Molded Device** Author(s) - Murali Sarangapani, Senthilkumar Balasubramanian, Eric Tan Swee Seng, Jason Wong Chin Yeung *Heraeus Materials Singapore Pte Ltd, Singapore | Senthilkumar.Balasubramanian@heraeus.com*
ID: 162	**Impact of lifetime and mechanical behaviors on TIM performance on high-end processor** Author(s) - Gamal Refai-Ahmed, Ho Hyung Lee, Hoa Do *Xilinx, United States of America | hohlee83@gmail.com*
ID: 166	**Mm-Wave Antenna in Package (AiP) Using Unbalanced Substrate with and without Solder Mask.** Author(s) - Kuan-Ta Chen, Bo-Siang Fang, Ying-Wei Lu, Chia-Chu Lai *SPIL, Taiwan* *guandachen@spil.com.tw*

ID: 178	**Discussion of the Signal Transmission Crosstalk** Author(s) - Yi Ting Tsou, I Huai Wang, Sung-Mao Wu *National University of Kaohsiung, Taiwan | wzo12345@gmail.com*
ID: 185	**Highly Stretchable, Durable, and Printable Textile Conductor** Author(s) - Won Jae Lee[1], Jin Yeong Park[1], Hyun Jin Nam[2], Sung-Hoon Choa[1] *[1]Graduate School of Nano IT Design Fusion, Seoul National University of Science and Technology, Seoul, 01811, Republic of Korea* *[2]Dept. Of Manufacturing System and Design Engineering Seoul National University of Science and Technology, Seoul, 01811, Republic of Korea* *shchoa@seoultech.ac.kr*
ID: 186	**Correlating Printing Performance of Solder Paste with Its Rheology** Author(s) - Saurabh Shrivastava, Ansuman Das, Sathiyanarayanan C *Alpha Assembly Solutions, A Macdermid Performance Solutions Business, India* *saurabh.shrivastava@alphaassembly.com*
ID: 191	**Laser hybrid integration on silicon photonic integrated circuits with reflected grating** Author(s) - Yu Sun[1,2], Man Zhao[1,2], Juan Wei[1,2], Fengman Liu[1,2], Haiyun Xue[1,2], Huimin He[1,2], Liqiang Cao[1,2] *[1]Institute of Microelectronics of Chinese Academy of Science,, China, People's Republic of* *[2]National Center for Advanced Packaging Co.,LTD (NCAP China), China,People's Republic of* *hehuimin@ime.ac.cn*
ID: 197	**Block-Based Finite Element Modeling, Simulation and Optimization of the Warpage of Embedded Trace Substrate** Author(s) - Chien-Yu Lien, Yao-Chen Chuang, Yuan Yao *National Tsing Hua University; s106032563@m106.nthu.edu.tw*
ID: 201	**The Balun Design by Embedding High Permittivity Material in The Substrate of CSP Package with Large Size** Author(s) - Ying-Wei Lu, Bo-Siang Fang, Hsuan-Hao Mi, Kuan-Ta Chen, Mike Tsai *Siliconware Precision Industries Co., Ltd., Taiwan | boxiangfang@spil.com.tw*
ID: 220	**Evaluating moldability challenges in a Large Strip Package with Transfer Molding Process simulation** Author(s) - Subramanian N.R. *Infineon Technologies Asia Pacific Pte Ltd, Singapore | Subramanian.N@infineon.com*
ID: 223	**Electrokinetic Behavior of Solder Powders in Non-aqueous Media** Author(s) - Terence Lucero Fernandez Menor, Manolo G. Mena, Herman D. Mendoza *University of the Philippines, Diliman | tfmenor@up.edu.ph*
ID: 226	**Effect of Bond Pad Surface Finish on AuSn Solder Bumping Using Laser Solder Jetting** Author(s) - Norhanani Jaafar, Chong Ser Choong *Institute of Microelectronics, Singapore | jaafarn@ime.a-star.edu.sg*
ID: 308	**Improvement of die shift by solder self-alignment for fan-out package process applications** Author(s) - Hwanpil Park, Sungchul Kim, Jae-Yong Park, Young-Ho Kim *Hanyang University, Korea, Republic of (South Korea) | Parkhwanpil@hanyang.ac.kr*

Interactive Session 2

Friday, 7th December
Room: Pisces
<10:20am - 11:10am> - <3:20pm - 3:40pm)

ID: 231	**A New Failure Mechanism of Inter Layer Dielectric Crack** Author(s) - Haiyan Liu, Xiangyang Li, Jun Li, Sean Xu *NXP, China, People's Republic of	Haiyan.liu@nxp.com*
ID: 233	**Package Level Warpage Simulation of Fan-Out Wafer Level Package Considering Visco-Elastic Material Properties** Author(s) - ZHAOHUI CHEN *IME A-Star, Singapore, Singapore	chenz@ime.a-star.edu.sg*
ID: 236	**Solution for Short Tail Issue on Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG) Bond Finger with 0.7mil Gold Wire** Author(s) - Leong Ching Wai, Teck Guan Lim *Institute of Microelectronics, Singapore	wailc@ime.a-star.edu.sg*
ID: 259	**Study on Ultra-thin & High-Pixel CMOS Image Sensor Module** Author(s) - Mark Huang, Huisheng Han, Huabin Wu, Chuangwen Huang, Weiqing Zhang *A-Kelon (Huizhou) Optronics Ltd., China, People's Republic of	mark_huang@a-kelon.com*
ID: 264	**Millimeter-wave resonator and cavity-back slot antenna in Fan-Out Wafer Level Packaging** Author(s) - Zihao Chen, Teck Guan Lim *Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research) chenzh89@gmail.com*
ID: 265	**Film Type PID Material** Author(s) - Toshizumi Yoshino, Toshimasa Nagoshi, Shuji Nomoto, Akihiro Nakamura *Hitachi Chemical, Japan	t-yoshino@hitachi-chem.co.jp*
ID: 273	**Fine pitch solder paste for advance packaging application** Author(s) - ruifen zhang *Heraeus material singapore, Singapore	ruifen.zhang@heraeus.com*
ID: 279	**A Complete Explanation of Warpage Behavior Across Backend Processes on Organic BGA in Strip Form and its Predictive Methodology** Author(s) - Jing-en Luan, Roseanne Duca *STMicroelectronics Pte Ltd, Singapore	jing-en.luan@st.com*
ID: 286	**Characterization and Performance of Ultrafine Lead-Free powders** Author(s) - Wei Chih Pan[1], Leng Hin Tan[1], Yee Ting Lo[1], Li San Chan[1], Sebastian Fritzsche[2] *[1]Heraeus Materials Singapore, Singapore [2]Heraeus Deutschland GmbH & Co. KG adrian.tan@heraeus.com*

ID: 287	**Mechanics of Copper Wire Bond Failure due to Thermal Fatigue** Author(s) - Stevan G Hunter[1,2], Subramani Manoharan[2], Patrick McCluskey[2] *[1]ON Semiconductor, United States of America [2]University of Maryland* *sputterman0@gmail.com*
ID: 290	**Surface planarization of polymeric interlayer dielectrics for FOWLP applications** Author(s) - Soojung Kang, Yejin Kim, Ayoung Moon, Sangwon Lee, Sarah Eunkyung Kim, Sungdong KIM *Seoul National University of Science and Technology, Korea, Republic of (South Korea)* *sj3163@naver.com*
ID: 296	**Investigation of solder void and packages crack defect in flip chip packaging by 3D computed tomography analysis.** Author(s) - Chin Yung Lai *Infineon, Malaysia | chinyung78@yahoo.com*
ID: 299	**Microstructure of Press-fit Connection and Its Impact on Board Level Reliability** Author(s) - Aruna Palaniappan[1], Li Li[2], Tae-Kyu Lee[1] *[1]Portland State University, United States of America [2]Cisco Systems, United States of America* *taeklee@pdx.edu*
ID: 313	**A Modified Unequal Wilkinson Power Divider Using T-Shaped Transformers** Author(s) - Ren-Fu Tsai, Pu-Hua Deng, Ting-Jung Chang *Department of Electrical Engineering, National University of Kaohsiung* *shadowuw90304@gmail.com*
ID: 317	**RDL Process Development of MEMS Wafer Level Chip Scale Packaging with Silicon Pillar/CuPd as Through Mold Interconnection** Author(s) - Boon Long Lau, Zhaohui Chen, Siak Boon Lim, Pei Siang Lim *IME astar, Singapore | laubl@ime.a-star.edu.sg*
ID: 320	**Power Integrity Analysis for Active Silicon Interposer** Author(s) - Zihao Chen, Teck Guan Lim *IME,A*STAR, Singapore | chenzh89@gmail.com*
ID: 321	**Characterization of PECVD of Amorphous Silicon Films from 150°C to 400°C** Author(s) - HOU JANG LEE *Institute of Microelectronics, Singapore | leehj@ime.a-star.edu.sg*
ID: 325	**Robust Packaging For MEMS Sensors Using Plastic Moulding** Author(s) - Guoqiang Wu, Leong Ching Wai, Daw Don Cheam, Peter Hyun Kee Chang, Navab Singh, Yuandong Gu *Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore* *changhk@ime.a-star.edu.sg*

ID: 337	**Face-up Interconnection Technique Using Direct Image Writing for Three-Dimensional Heterogeneous Flexible Electronics** Author(s) - Houngkyung Kim, Yongjin Kim, Jun Yeob Song, Jae Hak Lee, Seungman Kim *Korea Institute of Machinery & Meterials, Korea, Republic of (South Korea)* *houngkyung-kim@kimm.re.kr*
ID: 339	**Demonstration of Ultra-fine Pitch Au-Au Diffusion Bonding on Chip-on-Film (COF) with IGEPIG Surface Finishing** Author(s) - Pun Kelvin[1], Rotanson Jason[1], Chan Alan H.S[2] *[1]Compass Technology Co Ltd, Hong Kong S.A.R. (China)* *[2]City University of Hong Kong* *jason_rotanson@cgth.com*
ID: 344	**Effect of wire bonding on the performance of RFMEMS filters** Author(s) - Nan Wang, Yao Zhu, Teck Guan Lim, Navab Singh, Yuandong Gu *Institute of Microelectronics, Singapore	wangn@ime.a-star.edu.sg*
ID: 345	**A Lame Mode Resonator Based on Aluminum Nitride on Silicon Platform** Author(s) - Nan Wang, Yao Zhu, Guoqiang Wu, Zhipeng Ding, Eldwin Jiaqiang Ng, Nishida Yoshio, Peter Hyun Kee Chang, Navab Singh, Yuandong Gu *Institute of Microelectronics, Singapore	wangn@ime.a-star.edu.sg*
ID: 351	**Design and Modeling of Novel TSVs for Ternary Logic Applications** Author(s) - Ramesh Vobulapuram[1], Durga Prasad[1], Ramana Reddy[1], Divya Madhuri Badugu[2] *[1]Rajeev Gandhi Memorial College of Engineering and Technology, India* *[2]KL Deemed to be University* *divyamadhuri.badugu@gmail.com*
ID: 352	**A Novel Shielding Technique to Reduce the Crosstalk Effects in TSVs** Author(s) - Divya Madhuri, Sunitha Mani *KL University, India	divyamadhuri.badugu@gmail.com*
ID: 356	**Laser Drilling of Thru Mold Vias for FOWLP Application** Author(s) - Vasarla Nagendra Sekhar, David Soon Wee Ho, Srinivasa Rao Vempati, Ismael Cereno Daniel *Institute of Microelectronics, Singapore	vasarla@ime.a-star.edu.sg*
ID: 359	**A hybrid laser integration approach for miniature photonics sensors** Author(s) - JIFANG TAO, Ser Choong Chong, Tao Sun, Hong Cai, Navab Singh, Yuandong Gu *Institute of Microelectronics, Singapore	caih@ime.a-star.edu.sg*
ID: 360	**Solder Sphere Transfer for wafer level Packaging** Author(s) - Florian Bieck, Robert Thalmann, Christoph Glaubitz, Tom Friedrichson *PacTech Asia, Malaysia	florian.bieck@pactech.com*

Heterogeneous Integration Roadmap (HIR) Workshop EPTC 2018

Thursday, 6th December
<01:50pm - 06:00pm>
Gemini 1

Our Industry has reinvented itself through multiple disruptive changes in technologies, products and markets.. With the rapid migration of logic, memory and applications to the Cloud infrastructures, Data Centers and 5G Networks, the Internet of Things (IoT) to internet of everything (IOE), Autonomous Vehicles, the proliferation of Smart Devices every where, and increasing interest in artificial intelligence (AI) & Virtual Reality (VR) , the pace of innovation is increasing to meet these challenges. What are the paths forward?

The IEEE Heterogeneous Integration Technology Roadmap (HIR), is sponsored by the IEEE Electronic Packaging Society (EPS), the Electron Devices Society (EDS), Photonics Society together with ASME EPPD and SEMI. It will address the future directions of heterogeneous integration technologies and applications serving future markets and applications, so very crucial to our profession, our industries, academic and research communities. Following the spirit of ITRS, the HIR is a pre-competitive technology roadmap provides long-term vision to identify the needs of future technology challenges, roadblocks, and potential solutions focused on system integration and broad market applications in order to accelerate progress for the broad electronics industry.

Workshop Agenda

In this workshop we shall feature an introduction of the HIR followed by presentations from 5 of the 22 technical working groups (TWG)

* **Introduction**	**Andrew Tay**
* **Heterogeneous Integration Roadmap Overview**	**Bill Chen**
* **Wafer Level Packaging (WLP)**	**Rozalia Beica**
* **Thermal Management**	**Avram Bar-Cohen**
* **System in Package (SiP)**	**Rolf Aschenbrenner**
* **Electronics & Photonics Integration**	**Bill Bottoms**
* **Design & Simulation**	**Christopher Bailey**
* **Wrap-Up**	**Bill Bottoms & Bill Chen**

The Conference room will be available for further informal dialog & discussion until 6:30 pm

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Website:	www.amd.com

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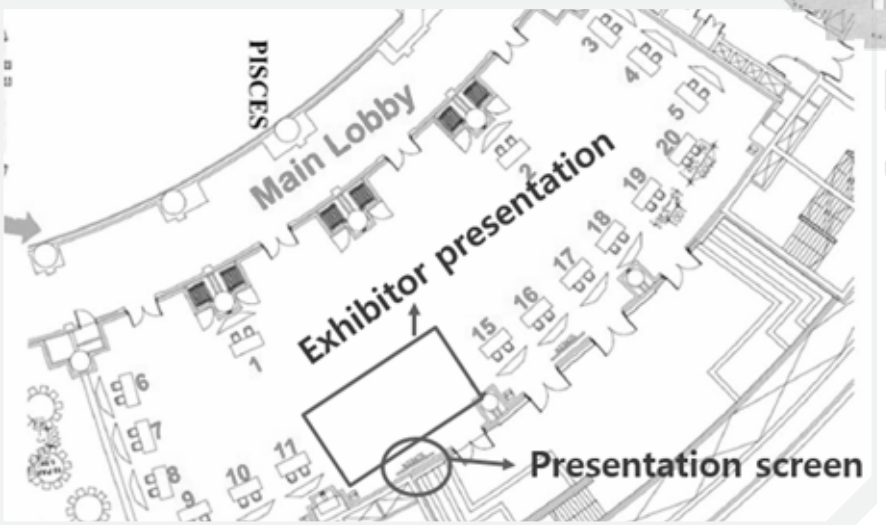

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Conference Venue

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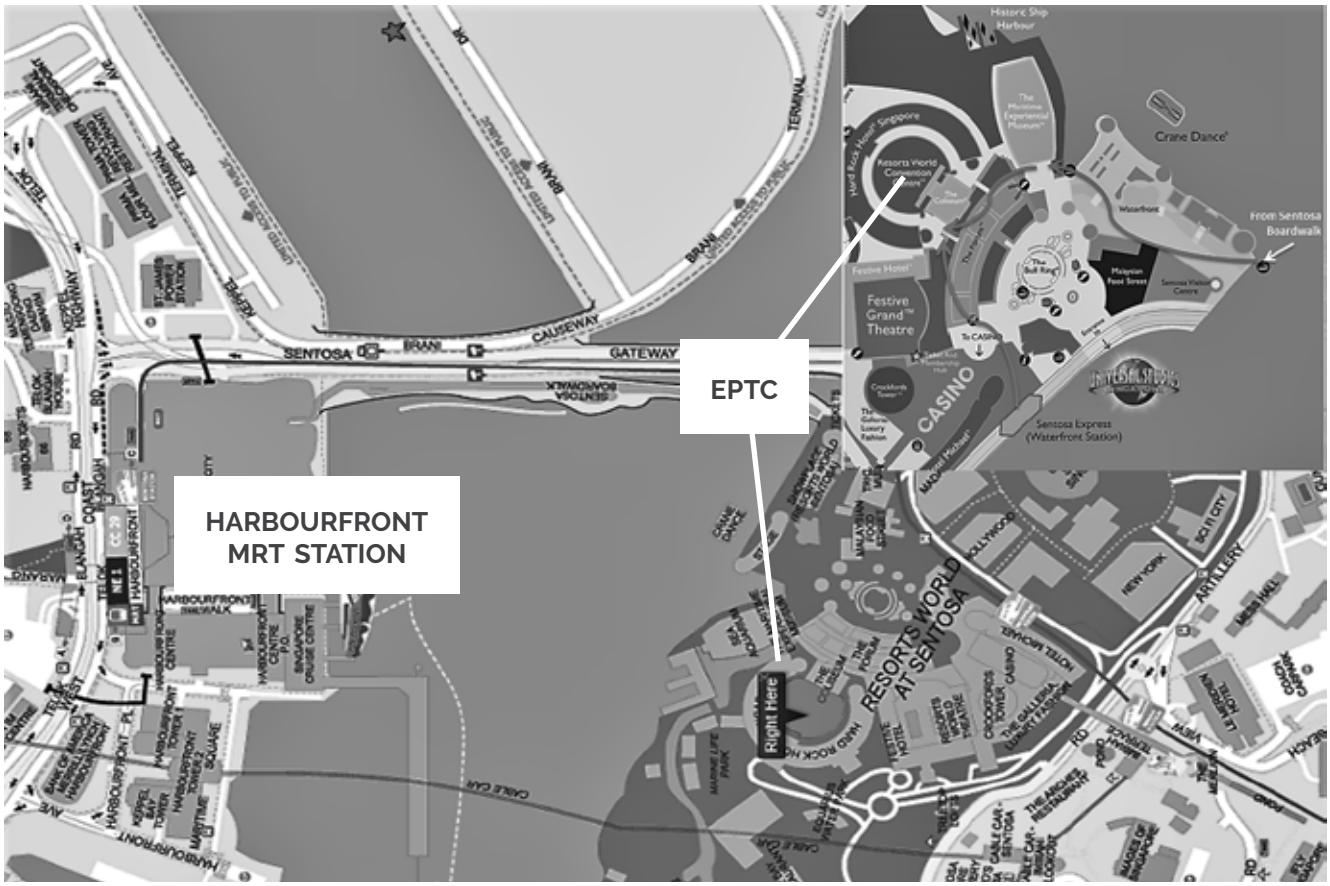
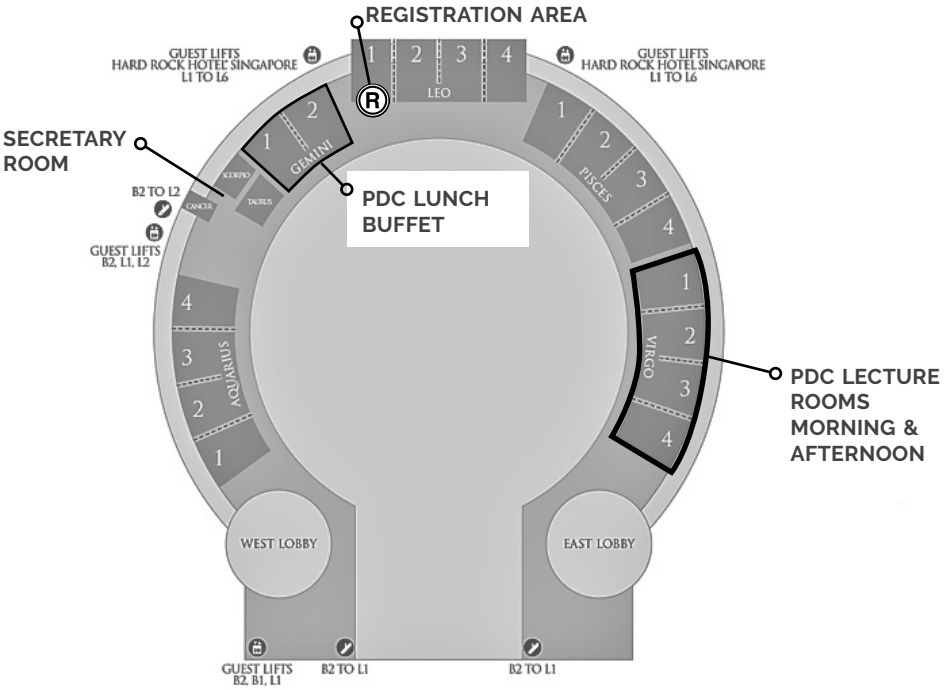


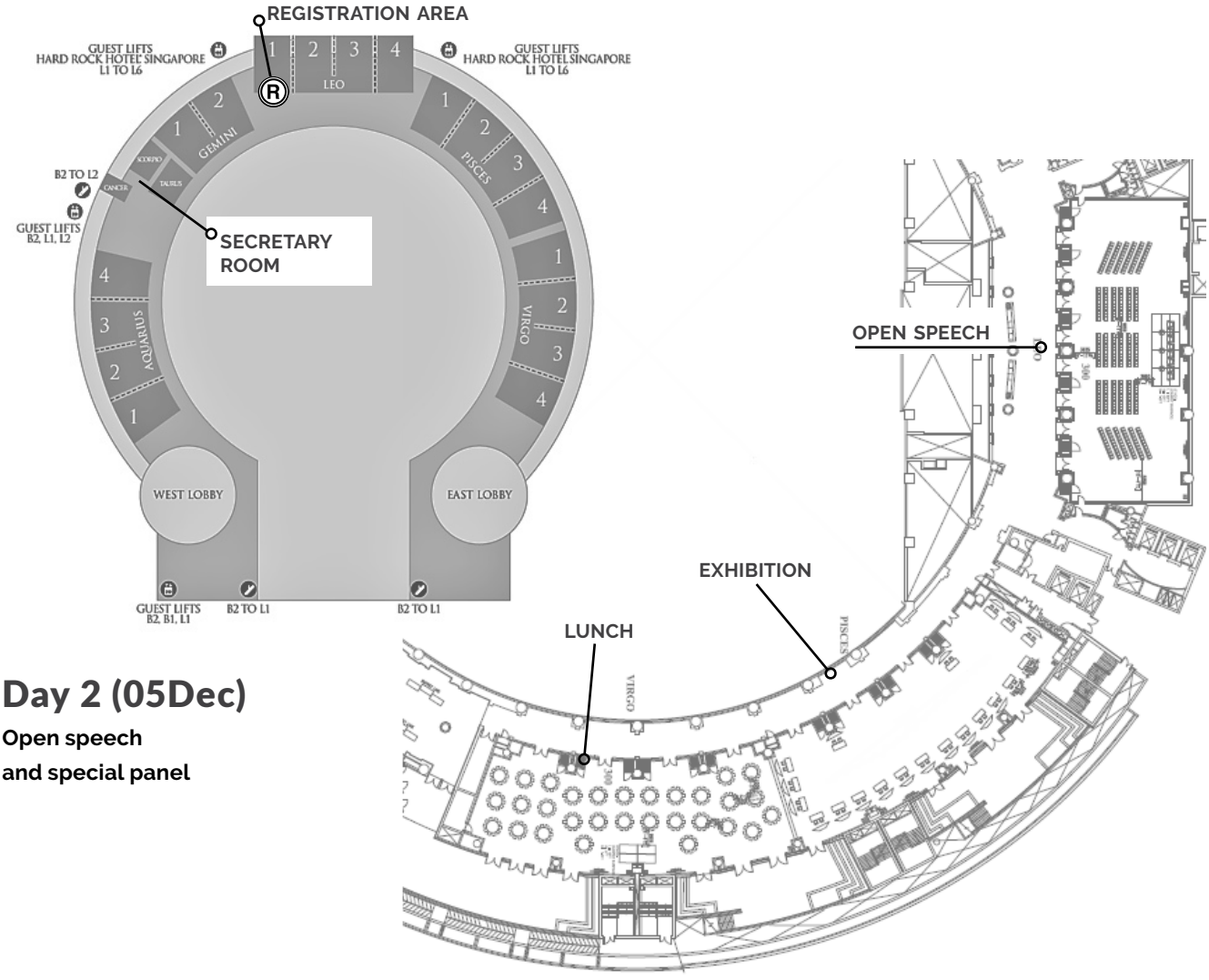
Day 1 (04Dec)

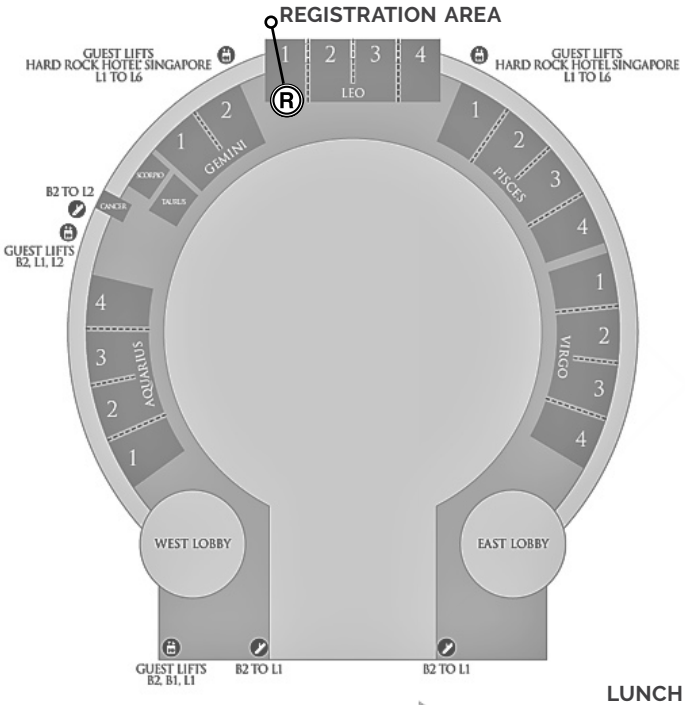
Professional Development Course

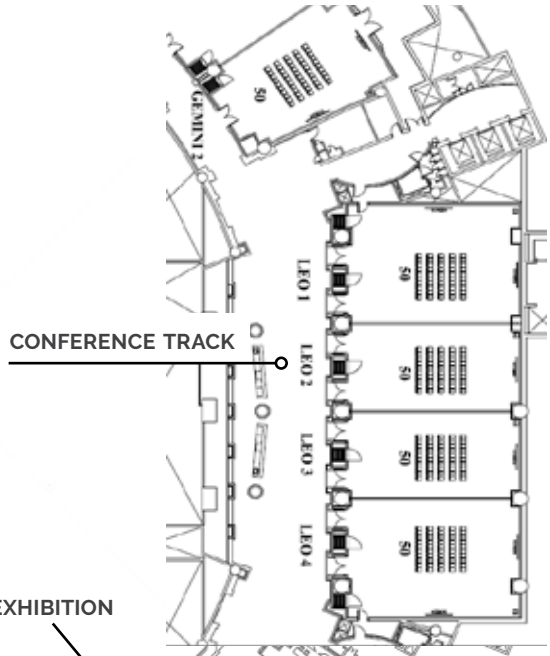


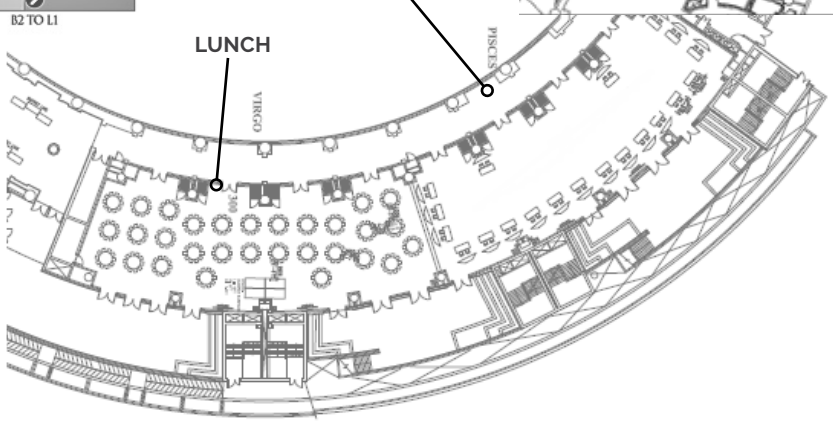
Day 2 (05Dec)

Open speech and special panel







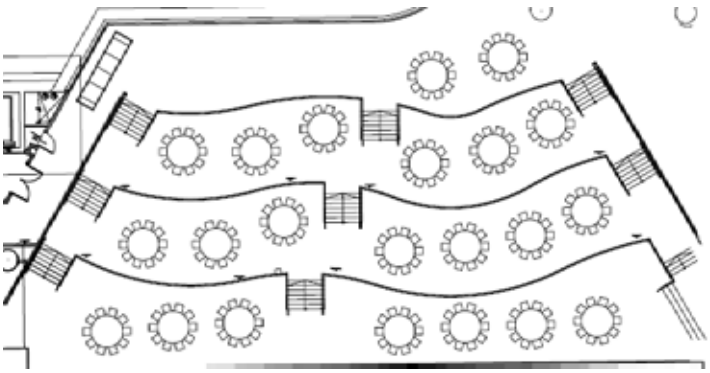


Day 3-4 (06-07Dec)

Conference Track

06 Dec

Banquet



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Do, Hoa	Xilinx Inc., United States of America	**A-05, G-05, Interactive Session 1**
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Du Bois, Bert	imec, Belgium	**A-09**
Duca, Roseanne	STMicroelectronics Pte Ltd, Singapore	**Interactive Session 2**
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Eibelhuber, Martin	EVGroup, Austria	**C-06**
Eichinger, Barbara	Infineon Technologies Austria Ag, Austria; Department Of Physics, University Of Graz, Graz, Austria	**A-12** Presenter
En, Yunfei	China Electronic Product Reliability And Environmental Testing Research Institute, People's Republic Of China	**D-12**
Engelsberger, Franz Xaver	Infineon Technologies, Germany	**G-17**
Fang, Bo-Siang	Siliconware Precision Industries Co., Ltd., Taiwan	**F-07** Presenter, **Interactive Session 1** Presenter

Author(s)	Organization(s)	Session
Farkas, Gabor	Mentor Graphics, Hungary	**Invited 20**
Feng, Huicheng	School of Mechanical and Aerospace Engineering, Nanyang Technological University, Singapore	**E-05, Interactive Session 1**
Feng, Qingming	IMTEK, University of Freiburg, Germany	**D-09**
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Ferrari, Philippe	RFIC-Lab, COMUE University, France	**C-11**
Flack, Warren W	Ultratech, a division of Veeco	**E-06**
Franke, Joerg	Friedrich-Alexander University Erlangen-Nürnberg, Germany	**E-07**
Franke, Joerg	Friedrich-Alexander University Erlangen-Nuremberg (FAU), Institute for Factory Automation and Production Systems (FAPS), Germany	**B-17**
Friedrichson, Tom	PacTech Asia, Malaysia	**Interactive Session 2**
Fries, Thomas	FRT GmbH, Bergisch-Gladbach, Germany	**B-15**
Fritzsche, Sebastian	Heraeus Deutschland GmbH & Co. KG	**Interactive Session 2**
Fu, Chao	WinTech Nano-Technology Services Pte. Ltd	**Interactive Session 1**
Fujiwara, Toshiya	Atotech Japan K.K.	**D-08**
Fulton, Stewart	SPTS Technologies Ltd, United Kingdom	**C-08** Presenter
Furuyama, Masaharu	FUJITSU LABORATORIES LTD., Japan	**B-05** Presenter
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Gantner, Eric	Intel Corporation	**C-14**
Garete, April Joy H.	Nexperia Philippines, Inc., Philippines	**A-08** Presenter
Glaubitz, Christoph	PacTech Asia, Malaysia	**Interactive Session 2**
Graham, Gabe	Lam Research, United States of America	**G-06**
Gu, Allen	ZEISS Semiconductor Manufacturing Technology, United States of America	**C-02**
Gu, Yuandong	ASTAR Institute of Microelectronics, Singapore	**Interactive Session 2**
Guerrieri, Stefano	Imec, Belgium	**G-11**
Guevara, Rafael Jose Lizares	Texas Instruments Phils, Philippines	**F-02, G-12**
Gunji, Keita	Nidec Read Corporation, Japan	**F-14** Presenter
Guntuku, Krishna Rao	Electro Optical Instruments Research Academy, Hyderabad, India	**F-12**
Guo, Fei	AMD, Singapore	**C-10**
Gupta, Mahender Kumar	Electro Optical Instruments Research Academy, Hyderabad, India	**F-12**
Gyenge, Oliver	MSG Lithoglas GmbH, Berlin, Germany	**C-09**
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Hagelauer, Amelie	Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany	**A-06**
Hall, Stephen	Intel Corporation	**C-14**
Hamasawa, Atsuhiro	KyushuUniversity/Japan, Japan	**G-04** Presenter
Hamelink, Johan	Boschman Technologies, Netherlands, The	**F-17**
Han, Huisheng	A-Kelon (Huizhou) Optronics Ltd., People's Republic of China	**Interactive Session 2**
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Ho, David Soon Wee	ASTAR Institute of Microelectronics, Singapore	**C-01, C-19, F-11, Interactive Session 1 & 2, E-16, G-16**
Hook, Michael	University of Waterloo, Canada	**A-02**
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Lee, Ho Hyung	Xilinx, United States of America	**Interactive Session 1**
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Lee, Tae-Kyu	Portland State University, United States of America	**Interactive Session 2**
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Lee, Yong-Woo	MKE, Korea, Republic of (South Korea)	**B-18**
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Li, Hui	Wuhan University, People's Republic of China China	**G-10**
Li, Jun	NXP, People's Republic of China	**Interactive Session 2**
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Li, Jun{Leo}	NXP Semiconductors, People's Republic of China	**A-03**
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Liao, Lois Jinzhi	WinTech Nano-Technology Services Pte. Ltd	**Interactive Session 1** Presenter
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Lien, Chien-Yu	National Tsing Hua University	**Interactive Session 1** Presenter
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Lim, Ming Siong	Infineon Technologies, Malaysia	**G-13**
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Lim, Siak Boon	Institute of Microelectronics, Singapore	**G-16**
Lim, Simon Siak Boon	Institute of Microelectronics, A*STAR, Singapore	**C-16, E-16, Interactive Session 2, F-01, F-11, D-10**
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Lim, Wei Lee	Infineon Technologies (Kulim) Sdn. Bhd, Malaysia	**C-07** Presenter
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Liu, Haiyan	NXP, People's Republic of China	**Interactive Session 2** Presenter
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Liu, Sheng	Wuhan University, People's Republic of China	**E-19, E-13**
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Lu, Ying-Wei	Siliconware Precision Industries Co., Ltd., Taiwan	**Interactive Session 1**
Luan, Jing-En	STMicroelectronics Pte Ltd, Singapore	**B-02, Interactive Session 2**
Ma, Shiyue	Tongji University, People's Republic of China China	**G-10**
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Majeed, Bivragh	imec, Belgium	**E-09**
Mamangun, Ruby Ann Dizon	Texas Instruments Phils, Philippines	**F-02, G-12**
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Mathew, John	National University of Singapore	**D-01** Presenter, **E-10**
Matthias, Thorsten	EVGroup, Austria	**C-06** Presenter
Maus, Simon	MSG Lithoglas GmbH, Berlin, Germany	**C-09**
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Nishikawa, Hiroshi	Osaka Univerisity, Japan	**Interactive Session 1**
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Nishimura, Tetsuro	Nihon Superior Co., Ltd., Japan	**E-18**
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Park, Chongmin	MK Electron Co., Ltd, Korea, Republic of (South Korea)	**E-17**
Park, Hae=Sung	Seoul National University of Science and Technology, Korea, Republic of (South Korea)	**Interactive Session 1** Presenter
Park, Jae-Yong	Hanyang University, Korea, Republic of (South Korea)	**Interactive Session 1**
Park, Jin Yeong	Graduate School of Nano IT Design Fusion, Seoul National University of Science and Technology, Seoul, 01811, Republic of Korea	**Interactive Session 1**
Pei Siang, Sharon Lim	Institute of Microelectronics, Singapore	**C-15**
Peng, Juan	Wuhan University of Technology, People's Republic of China	**E-13**
Pham, Nga Phuong	imec, Belgium	**A-09** Presenter
Philofsky, Brian	Xilinx Inc., United States of America	**G-05**
Phua, Eric Jian Rong	School of Materials Science and Engineering; School of Chemical and Biomedical Engineering	**F-08** Presenter
Pi, Yudan	School of Electronic and Computer Engineering, Peking University Shenzhen Graduate School, Shenzhen, Guangdong, China; Institute of Microelectronics, Peking University, Beijing, China	**E-20**
Pistono, Emmanuel	RFIC-Lab, COMUE University, France	**C-11**
Plomantes, Jose Arvin Matute	Texas Instruments Phils, Philippines	**F-02, G-12**
Podevin, Florence	RFIC-Lab, COMUE University, France	**C-11**
Ponnuswamy, Thomas	Lam Research, United States of America	**G-06**
Poppe, Andras	Mentor Graphics, Hungary; Budapest University of Technology and Economics, Hungary	**Invited 20**
Prasad, Durga	Rajeev Gandhi Memorial College of Engineering and Technology, India	**Interactive Session 2**
Qi, Feng	Intel	**D-16** Presenter
Qin, Ivy	kulicke and soffa ind. inc, United States of America	**E-02**
Quandt, Stefan	Trumpf, Inc., United States of America	**D-03**
Radhamony, Rahul Babu	Qualcomm, Inc., USA	**C-12**
Raju, Salahuddin	Institute of Microelectronics, A*STAR, Singapore	**C-19**
Ramasamy, Anandan	Xilinx Asia Pacific Ltd, Singapore	**B-01** Presenter
Ramona, Ramona	ASTAR Institute of Microelectronics, Singapore	**E-14, G-09**
Ranjith, Kandasamy	Nanyang Technological University, Singapore	**Interactive Session 1**
Raszkowski, Tomasz	Lodz University of Technology, Poland	**D-06** Presenter
Ravinder, Pal Singh	Institute of Microelectronics, Singapore	**B-06**
Reddy, Ramana	Rajeev Gandhi Memorial College of Engineering and Technology, India	**Interactive Session 2**
Refai-Ahmed, Gamal	Xilinx, United States of America	**Interactive Session 1, A-05, G-05**
Ren, Qin	Institue of Microelectronics, A*star, Singapore	**E-01** Presenter

Author(s)	Organization(s)	Session
Rencz, Marta	Mentor Graphics, Hungary; Budapest University of Technology and Economics, Hungary	**Invited 20**
Ridremont, Romain	JSR MICRO NV	**E-06**
Rimböck, Johanna	EVGroup, Austria	**C-06**
Roellig, Mike	Fraunhofer Institute for Ceramic Technologies and Systems IKTS, Germany	**B-07**
Rongen, Rene	NXP Manufacturing (Thailand) Ltd, Thailand	**C-17**
Roscain, Reinald John S.	Nexperia Philippines, Inc., Philippines	**A-08**
Rzepka, Sven	Fraunhofer Institute for Electronic Nano Systems ENAS, Technologie-Campus 3, 09126; Fraunhofer ENAS, Dept. Micro Materials Center, Chemnitz, Germany;	**B-15, F-10**
Sabuncuoglu, Deniz	imec, Belgium	**A-09**
Sakamoto, Mamoru	Kyushu University, Japan	**D-18**
Salam, Budiman	Singapore Institute of Manufacturing Technology, Singapore	**D-14** Presenter, **Interactive Session 1**
Samson, Agnieszka	Lodz University of Technology, Poland	**D-06**
Sarangapani, Murali	Heraeus Materials Singapore Pte Ltd, Singapore	**Interactive Session 1**
Sardana, Nitesh Kumar	Robert Bosch Engineering and Business Solution Pvt Ltd, India	**Interactive Session 1** Presenter
Sawano, Mitsuru	FUJIFILM Corporation, Japan	**F-06**
Sayama, Toshihiko	Machinery & Electronics Research Institute, Toyama Industrial Technology Development Center, Japan	**G-08**
Scheetz, Matthias	Friedrich-Alexander University Erlangen-Nürnberg, Germany	**E-07**
Schmidbauer, Philipp	Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany	**A-06** Presenter
Schmitt, Wolfgang	Heraeus Deutschland GmbH & Co. KG, Germany	**B-08**
Schulze, Gary	kulicke and soffa ind. inc, United States of America	**E-02**
Schwarzer, Christian	Aschaffenburg University of Applied Science	**E-07**
Seiler, Bettina	CWM GmbH, Chemnitz, Germany	**B-15**
Seit, Wen Wei	IME, Singapore	**C-16, G-02**
Sekhar, Vasarla Nagendra	Institute of Microelectronics, A*STAR, Singapore	**D-17, F-01, Interactive Session 2** Presenter
Ser Choong, Chong	Institute of Microelectronics, Singapore	**Interactive Session 1**
Shah, Aashish	kulicke and soffa ind. inc, United States of America	**E-02**
Shan, Xuechuan	Singapore Institute of Manufacturing Technology, Singapore	**D-14, Interactive Session 1**
Shang, Yang	Advantest (Singapore) Pte Ltd, Singapore	**C-12** Presenter
Shekhar, Sameer	Intel Corporation, Hillsboro, USA	**B-04, C-05**
Shen, Shengnan	\Wuhan University, People's Republic of China China	**G-10**
Shen, Zhipeng	Quzhou University, People's Republic of China	**G-20**
Shi, Tielin	Huazhong University of Science and Technology, People's Republic of China	**E-12**
Shimada, Kazuto	FUJIFILM Corporation, Japan	**F-06**
Shinohara, Makoto	Advantest Corporation, Japan	**C-12**
Shrivastava, Kratika	Robert Bosch Engineering and Business Solution Pvt Ltd, India	**Interactive Session 1**
Shrivastava, Saurabh	Alpha Assembly Solutions, A Macdermid Performance Solutions Business, India	**Interactive Session 1** Presenter
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Singh, Shiv Govind	Indian Institute of Technology Hyderabad, India	**F-18, G-07**

Author(s)	Organization(s)	Session
Slabbekoorn, John	IMEC	**E-06**
Soestbergen, Michiel Van	NXP Manufacturing (Thailand) Ltd, Thailand	**C-17**
Soh, Serine	Institute of Microelectronics, A*STAR, Singapore	**C-19, F-11**
Son, Jae-Yeol	MKE, Korea, Republic of (South Korea) ; Sungkyunkwan University, Korea, Republic of (South Korea)	**B-18**
Song, Changmin	Seoul National University of Science and Technology, Korea, Republic of (South Korea)	**Interactive Session** 1 Presenter
Song, Jun Yeob	Korea Institute of Machinery & Meterials, Korea, Republic of (South Korea)	**Interactive Session 2**
Sreerama, Chaitanya	Intel Corporation	**C-14**
Stefenelli, Mario	Infineon Technologies Austria AG, Austria	**C-07**
Stoyanov, Stoyan	University of Greenwich, United Kingdom	**B-10**
Su, Deqi	Quzhou University, People's Republic of China	**G-20**
Su, Meiying	Institute of microelectronics of Chinese academy of sciences; The National Center for Advanced Packaging, People's Republic of China	**D-07** Presenter, **D-20** Presenter
Subbiah, Nilavazhagan	IMTEK, University of Freiburg, Germany	**D-09** Presenter
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Suhard, Samuel	IMEC	**E-06**
Sun, Tao	Institute of Microelectronics, Singapore	**Interactive Session 2**
Sun, Yu	Institute of Microelectronics of Chinese Academy of Sciences; National Center for Advanced Packaging Co.LTD	**G-14, Interactive Session 1**
Suzuki, Naoya	Hitachi Chemical Co.,Ltd., Japan	**F-16**
Sweatman, Keith	Nihon Superior Co., Ltd., Japan	**E-18**
Tan, Chuan Seng	Nanyang Technological University, Singapore	**D-19**
Tan, Lee Siew Rachel	Singapore Institute of Manufacturing Technology, Singapore	**Interactive Session 1**
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Tang, Wenbin	School of Mechanics, Civil Engineering and Architecture, Northwestern Polytechnical University, Xi'an, China	**F-20, Interactive Session 1**
Tang, Xudong	Intel	**D-16**
Tang, Zirong	Huazhong University of Science and Technology, People's Republic of China	**E-12**
Tao, Jifang	Institute of Microelectronics, Singapore	**Interactive Session 2**
Tao, Jing	Nanyang Technological University, Singapore	**D-19** Presenter
Tasaki, Takashi	ARAKAWA CHEMICAL INDUSTRIES, LTD., Japan	**C-13**
Teo, Lingling	heraeus material Singapore	**C-18**
Tetsushi, Fujinaga	ULVAC	**B-16**
Thalmann, Robert	PacTech Asia, Malaysia	**Interactive Session 2**
Tianqing, Wu	National University of Singapore	**D-01**
Tilford, Tim	University of Greenwich, United Kingdom	**B-10**
Toh, Kok Chuan	School of Mechanical and Aerospace Engineering, Nanyang Technological University, Singapore	**E-05, Interactive Session 1**
Tolunay Wipf, Selin	IHP, Germany	**C-11**
Torza, Anthony	Xilinx Inc., United States of America	**G-05**
Tsai, Cheng-Yu	Advanced Semiconductor Engineering, Inc, Taiwan	**C-20**

Author(s)	Organization(s)	Session
Tsai, Jensen	Siliconware Precision Industries Co., Ltd., Taiwan	**A-01**
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Tsai, Ren-Fu	Department of Electrical Engineering, National University of Kaohsiung	**Interactive Session 2** Presenter
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Tsou, Yi Ting	National University of Kaohsiung, Taiwan	**Interactive Session 1** Presenter
Tsugami, Kota	Kyushu University, Japan	**B-09** Presenter
Tsuritani, Hiroyuki	Machinery & Electronics Research Institute, Toyama Industrial Technology Development Center, Japan	**G-08**
Uesugi, Kentaro	SPring-8, Japan Synchrotron Radiation Research Institute (JASRI)	**G-08**
Uhrmann, Thomas	EVGroup, Austria	**C-06**
Umar, Zeeshan	Infineon Technologies, Germany	**G-17**
Umemoto, Taku	LINTEC Advanced Technologies (Europe) GmbH	**C-08**
V C Muniandy, Kesvakumar	Infineon Technologies Asia Pacific Pte Lte, Singapore	**B-03** Presenter
Van Acker, Lut	imec, Belgium	**E-09**
Van Hoof, Rita	imec, Belgium	**A-09**
Van Lijnschoten, Bert	Imec, Belgium	**G-11**
Vanjari, Siva Rama Krishna	Indian Institute of Technology Hyderabad, India	**F-18, G-07**
Vasarla, Nagendra Sekhar	Institute of Microelectronics, Singapore	**B-16** Presenter
Vempati, Srinivasa Rao	Institute of Microelectronics, Singapore	**B-16, Interactive Session 2**
Vobl, Matthias	Infineon Technologies, Am Campeon 1-15, 85579 Neubiberg, Germany	**F-10**
Vobulapuram, Ramesh	Rajeev Gandhi Memorial College of Engineering and Technology, India	**Interactive Session 2**
Voß, Thomas	IHP, Germany	**C-11**
Wai, Leong Ching	Institute of Microelectronics, A*STAR, Singapore	**B-06, D-04, G-16, Interactive Session 2**
Wai Leong Ching, Eva	Institute of Microelectronics, A*STAR, Singapore	**B-13**
Wang, Bei	University of Applied Sciences Berlin, Germany	**C-09**
Wang, Bisheng	Huawei Technologies Co Ltd	**Interactive Session 1**
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Wang, Miaocao	Huzahong University of Science and Technology, People's Republic of China	**E-19**
Wang, Nan	Institute of Microelectronics, Singapore	**Interactive Session 2** Presenter
Wang, Shanda	Loughborough University, United Kingdom	**D-02**
Wang, Wei	Institute of Microelectronics, Peking University, Beijing, China; National Key Lab of Micro/Nano Fabrication Technology, Peking University, Beijing, China 1	**E-20**
Wang, Xiang Yu	Institute of Microelectronics (IME), A*STAR (Agency for Science, Technology and Research), Singapore	**E-01, Interactive Session 1** Presenter
Wang, Xiaobai	Institute of Materials Research and Engineering, Singapore	**A-13, E-03, F-15,**
Wang, Yu-Po	SPIL, Taiwan	**A-01**
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Author(s)	Organization(s)	Session
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Whalley, David	Loughborough University, United Kingdom	**D-02**
Wickramanayaka, Sunil	Institute of Microelectronics, A*STAR, Singapore	**D-17**
Wiesenhuetter, Felix	Hegewald & Peschke Mess- und Prueftechnik GmbH	**B-07**
Wietstruck, Matthias	IHP, Germany	**C-11** Presenter
Wilde, Jürgen	IMTEK, University of Freiburg, Germany	**D-09**
Winderickx, Gillis	imec, Belgium	**A-09**
Wing, Leong Yew	Institute of Microelectronics, A*STAR, Singapore	**C-19**
Winkle, Casey	Intel	**D-16**
Wipf, Christian	IHP, Germany	**C-11**
Wojnowsk, Maciej	Infineon Technologies, Germany	**G-17**
Wojnowski, Maciej	Infineon Technologies AG	**A-06**
Wong, Nelson	kulicke and soffa ind. inc, United States of America	**E-02**
Wong, Teck Neng	School of Mechanical and Aerospace Engineering, Nanyang Technological University, Singapore	**E-05, Interactive Session 1**
Wong, Wui Weng	AMD, Singapore	**C-10**
Wong Chin Yeung, Jason	Heraeus Materials Singapore Pte Ltd, Singapore	**Interactive Session 1**
Wrona, Jerzy	Singulus Technologies, Kahl am Main, Germany	**C-19**
Wu, Alan	Qualcomm, Inc., USA	**C-12**
Wu, Guoqiang	Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore;	**Interactive Session 2**
Wu, Huabin	A-Kelon (Huizhou) Optronics Ltd., People's Republic of China	**Interactive Session 2**
Wu, Peiyan	Space Research Institute of Electronics and Information Technology, Aerospace Science and Technology Corporation, Xi'an, China	**Interactive Session 1**
Wu, Sung-Mao	National University of Kaohsiung, Taiwan	**Interactive Session 1**
Wu, Tianqing	National University of Singapore	**E-10**
Xie, Hongyu	Institute of Microeclectronics, Singapore	**F-03**
Xie, Ling	Institute of Microelectronics, A*STAR, Singapore	**D-17** Presenter, **F-03**
Xu, Sean	NXP, People's Republic of China	**Interactive Session 2**
Xu, Yixin	Huzahong University of Science and Technology, People's Republic of China	**E-19** Presenter
Xue, Haiyun	Institute of Microelectronics of Chinese Academy of Sciences; National Center for Advanced Packaging Co.LTD	**G-14, Interactive Session 1**
Yacoub-George, Erwin	Fraunhofer EMFT Research Institution for Microsystems and Solid State Technologies, Munich, Germany	**C-04**
Yamamoto, Kazunori	Institute of Microelectronics, Singapore	**B-06, B-16**
Yang, Dengfeng	The National Center for Advanced Packaging, People's Republic of China	**D-07**
Yang, Ling	Sandisk/Western Digital, People's Republic of China	**Interactive Session 1**
Yao, Bin	China electronic product reliability and environmental testing research institute, People's Republic of China	**D-12**
Yao, Yao	School of Mechanics, Civil Engineering and Architecture, Northwestern Polytechnical University, Xi'an, China	**F-20, Interactive Session 1**

Author(s)	Organization(s)	Session
Yao, Yuan	National Tsing Hua University	**Interactive Session 1**
Yap, Christopher	National University of Singapore	**D-01**
Ye, Yong Liang	Institute of Microelectronics, Singapore	**B-06**
Yong, Khang Choong	Intel Corporation; Intel Microelectronics Sdn Bhd, Malaysia	**C-14, F-09**
Yoon, Jeong-Won	Korea Institute of Industrial Technology (KITECH), Korea, Republic of (South Korea)	**C-03**
Yoon, Jin-Ho	Ntrium Inc., Korea, Republic of (South Korea)	**G-19**
Yoon, Seung	Statschippac PTE LTD, JCET Group, Singapore	**E-11** Presenter
Yoshino, Toshizumi	Hitachi Chemical, Japan	**Interactive Session 2** Presenter
Yoshio, Nishida	Institute of Microelectronics, Singapore	**Interactive Session 2**
Yoshiteru, Takaya	SCREEN Finetech Solutions Co., Ltd.	**B-16**
Yu, Sijia	Quzhou University, People's Republic of China	**G-20**
Zenger, Tobias	EVGroup, Austria	**C-06**
Zhang, David Wei	School of Microelectronics, Fudan University	**D-07**
Zhang, Lidong	NXP Semiconductors, People's Republic of China	**A-03**
Zhang, Mengjia	Robert Bosch GmbH, Automotive Electronics, Reutlingen, Germany	**B-15**
Zhang, Ruifen	heraeus material Singapore	**C-18** Presenter, **Interactive Session 2**
Zhang, Weiqing	A-Kelon (Huizhou) Optronics Ltd., People's Republic of China	**Interactive Session 2**
Zhang, Wenqi	Institute of microelectronics of Chinese academy of sciences; The National Center for Advanced Packaging, People's Republic of China	**D-07**
Zhang, Xiaobing	Harbin Institute of Technology Shenzhen Graduate School, People's Republic of China	**Interactive Session 1**
Zhang, Xiaowu	Institute of Microelectronics, Singapore; IME, Singapore; IME A*STAR, Singapore	**A-13, A-15, B-06, C-16, D-10, D-11, E-03, E-15, F-15, Interactive Session 1**
Zhang, Yuanxiang	Quzhou University, People's Republic of China	**G-20** Presenter
Zhang, Yucheng	Technische Universität Berlin, Germany; Fraunhofer Institute for Reliability and Microintegration, Germany	**C-09**
Zhang, Zheng	Institute of Scientific and Industrial Research, Osaka university, Japan	**A-07** Presenter
Zhao, Man	Institute of Microelectronics of Chinese Academy of Science,, People's Republic of China; National Center for Advanced Packaging Co.,LTD (NCAP China)	**Interactive Session 1**
Zhou, Bin	China Electronic Product Reliability And Environmental Testing Research Institute, People's Republic Of China	**D-12**
Zhou, Cheng	Space Research Institute of Electronics and Information Technology, Aerospace Science and Technology Corporation, Xi'an, China	**Interactive Session 1**
Zhou, Xing	Harbin Institute of Technology Shenzhen Graduate School, People's Republic of China	**Interactive Session 1**
Zhu, Fulong	Huzahong University of Science and Technology, People's Republic of China	**E-19**
Zhu, Yao	Institute of Microelectronics, Singapore	**Interactive Session 2**
Zubert, Mariusz	Lodz University of Technology, Poland	**D-06**

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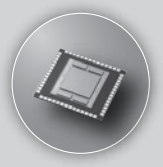
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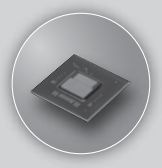
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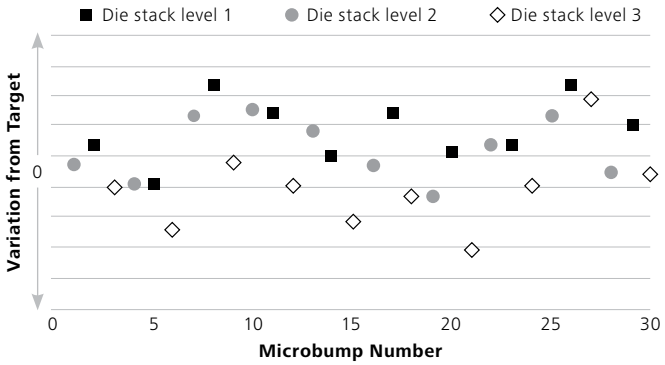

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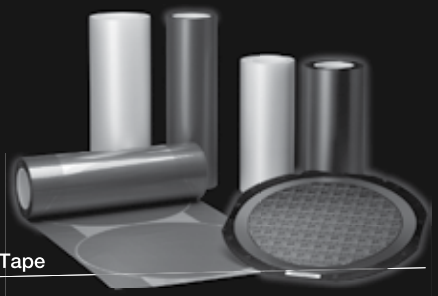

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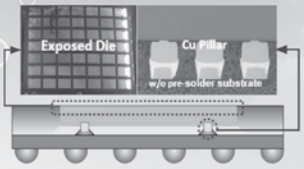
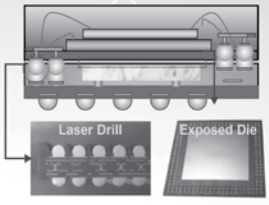
(Exposed Die+Cu pillar bump)



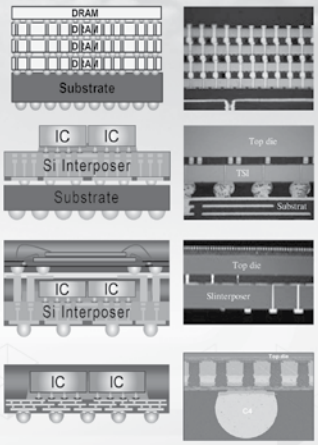
CuFCBGA
(Cu pillar bump)

HBW memory PoP
(High bandwidth)

ED-CuFC-ePoP
(Enhanced PKG on PKG)

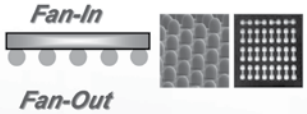


3D-IC

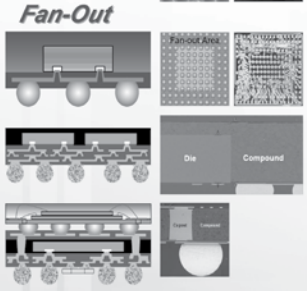


Wafer Level Package

Fan-In

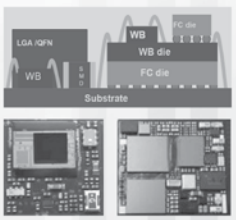


Fan-Out



Advanced Wire Bonding
(Cu wire / Ag wire)

SiP Module



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(Embedded Trace Substrate)

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EPTC 2018 PROGRAM OVERVIEW

TUESDAY, 4TH DECEMBER

07:30am-08:30am	**Registration at Leo 1's Foyer**		
08:30am-12:00pm	**PDC 01: Introduction to Fan-out Wafer Level Packaging** - Dr. Beth Keser	**PDC 02: Advanced Integrated Circuit Design for Reliability** - Dr. Richard Rao	**PDC 03: 3D SIP For ASIC and DRAM Integration** - Dr. Li Li
12:00pm-01:30pm	**Lunch**		
01:30pm-05:00pm	**PDC 04: Understanding Flip Chip Technology and Its Applications** - Mr. Eric Perfecto	**PDC 05: Introduction to 3D Interconnect and Packaging Technologies** - Prof. Sarah Kim	**PDC 06: Power Electronic Packaging Reliability, Materials, Assembly and Simulation** - Dr. Ning-Cheng Lee / Dr. Yong Liu / Prof. Sheng Liu
	Virgo 1	Virgo 2	Virgo 3

WEDNESDAY, 5TH DECEMBER

08:00am-08:45am	**Registration at Leo 1's Foyer**	
08:45am-09:30am	**Opening Ceremony**	Leo 1-2-3-4
09:30am-10:15am	**Keynote 01: Mr. Ivor Barber, Vice President, Packaging Engineering, AMD.**	
10:15am-10:45am	**Coffee/Tea Break** at Pisces Room	
10:45am-11:30am	**Keynote 2: Dr. Avram Bar-Cohen, Principal Engineering Fellow at Raytheon Corporation and Life Fellow of IEEE.**	Leo 1-2-3-4
11:30am-12:15pm	**Keynote 3: Ms Jean Trewhella , Director, Packaging Test, Development and Operations, GLOBALFOUNDRIES.**	
12:00pm-01:30pm	**EPS Luncheon** at Virgo Room	
01:30pm-03:30pm	**Plenary Session 1: Heterogeneous Packaging** - Dr. William Chen (Moderator) Dr. Gamal Refai-Ahmed | Mr. Mike Delaus | Mr. Manish Ranjan | Dr. Yu-Po Wang	Leo 1-2-3-4
03:30pm-04:00pm	**Coffee/Tea Break** at Pisces Room	
04:00pm-06:00pm	**Plenary Session 2: Packaging for next generation automobiles/autonomous cars** - Dr. Yoon Seung (Moderator) Mr. Gaurab Majumdar | Ms. LC Tan | Mr. Christophe Bouquet | Mr. Santosh Kumar	Leo 1-2-3-4
06:00pm-08:00pm	**VIP Dinner**	

THURSDAY, 6TH DECEMBER

	Gemini 2	Leo 1	Leo 2	Leo 3	Leo 4
08:30am-09:00am	**Invited #1 : Mr.Sam Karikalan**	**Invited #2 : Prof. Tan Chuan Seng**	**Invited #3 : Ms. Lim Sze Pei**	**Invited #4 : Dr. Gokul Kumar**	**Invited #5 : Prof. Robert Kao**
09.00am-10.00am A01-A15	**Advanced Packaging I**	**Interconnect Technologies I**	**Materials and Processing I**	**Emerging Technologies I**	**Thermal Characterization & Cooling Solutions I**
10:00am-11:00am	**Tea/Coffee Breaks-03: Interactive Session I and Exhibitor Presentation 1** at Pisces Room				
11.00am-12.20pm B01-B20	**Advanced Packaging II**	**Quality, Reliability & Failure Analysis I**	**Materials and Processing II**	**Electrical Simulation & Characterization I**	**Mechanical Simulation & Characterization I**
12:20pm-01:50pm	**Lunch-03: Best paper Award, EPTC 2018 committee Appreciation** at Virgo Room				
01:50pm-02:20pm	**Invited #6 : Dr. Han-Ping Pu**	**Invited #7 : Dr. Kedar Hardikar**	**Invited #8: Dr.Dongshun Bai**	**Invited #9: Dr.Tanja Braun**	**Invited #10 : Dr. Stevan Hunter**
02:20pm-03:40pm C01-C20	**TSV & WLB Packaging I**	**Quality, Reliability & Failure Analysis II**	**Materials and wProcessing III**	**Emerging Technologies II**	**Electrical Simulation & Characterization II**
03:40pm-04:40pm	**Coffee/Tea break & Interactive Session 1 Exhibitor Presentation 2** at Pisces Room				
04:40pm-06:00pm D01 - D20	**Thermal Characterization & Cooling Solutions II**	**Interconnect Technologies II**	**Materials and Processing IV**	**Emerging Technologies III**	**Mechanical Simulation & Characterization II**
01:50pm-06:00pm	**Heterogeneous Integration Roadmap Workshop** (Parallel Session to Technical paper tracks) at Gemini 1 Room				
06:30pm-09:30pm	**Conference Banquet**				

FRIDAY, 7TH DECEMBER

08:30am- 09:00am	**Invited #11 : Mr. Santosh Kumar**	**Invited #12 : Prof. David Harvey**	**"Invited #13: Mr. Shunsuke Tonouchi"**	**Invited #14 : Ms.Rozalia Beica**	**Invited #15 Prof. Andrew Tay**
09.00am-10.20am E01 - E20	**TSV & WLB Packaging II**	**Interconnect Technologies III**	**Materials and Processing V**	**Emerging Technologies IV**	**Thermal Characterization & Cooling Solutions III**
10:20am-11:10am	**Tea/Coffee Breaks-05: Interactive Session 2 / Exhibitor Presentation 3** at Pisces Room				
11.10am-12.30pm F01 - F20	**Advanced Packaging III**	**Equipment and Process Automation**	**Materials and Processing VI**	**Electrical Simulation & Characterization III**	**Mechanical Simulation & Characterization III**
12:30pm-01:30pm	**Lunch-03: EPTC 2019 Introduction: Sponsors Appreciation** at Virgo Room				
01:30pm-02:00pm	**Invited #16: Mr. Minwoo Daniel Rhee**	**Invited #17 Mr.Kei Murayama**	**Invited #18: Prof. Jeff Suhling**	**Invited #19 : Dr.Bill Bottoms**	**Invited #20 : Prof. Marta Rencz**
02:00pm- 03:20pm G01 - G20	**TSV & WLB Packaging III**	**Interconnect Technologies IV**	**Quality, Reliability & Failure Analysis III**	**Emerging Technologies V**	**Thermal simulation and modeling IV**
03:20pm-03:40pm	**Tea/Coffee Breaks-06: Interactive Session 2** at Pisces Room				
03:40pm-05:40pm	**Plenary Session 3: Next Generation Packaging Technologies -** Mr. Shigenori Aoki (Moderator) Dr. Yasumitsu Orii | Mr. Yasushi Masuda | Dr. Hideyuki Nasu | Dr. Toshihisa Nonaka				Virgo
05:40pm-06:00pm	**Closing Ceremony: Lucky Draw**				